

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
EDWARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

SQT 42

FACILITY FORM 602

N67-28825	
(ACCESSION NUMBER)	(THRU)
67	1
(PAGES)	(CODE)
CR-84841	14
(NASA CR OR TMX OR AD NUMBER)	(CATEGORY)

ARACON GEOPHYSICS CO.
DIVISION OF ALLIED RESEARCH ASSOCIATES, INC.
CONCORD, MASSACHUSETTS

**ARACON PHOTOGRAMMETRIC ATTITUDE
SYSTEM HARDWARE DESCRIPTION
AND
MAINTENANCE MANUAL**

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JULY 1965

CONTRACT NO. NAS5-3953

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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FOREWORD

This document is meant as a special-purpose adjunct to the comprehensive System Description.¹ For a detailed discussion of operator instructions see the Operator's Manual.²

¹ Wood, T. F., 1965: ARACON Photogrammetric Attitude System Description, Technical Report No. 1, Contract No. NAS5-3953, ARACON Geophysics Company.

² Wood, T. F. and C. R. Jones, III, 1965: TIROS Wheel Photogrammetric Attitude Operator's Manual, Technical Report No. 2, Contract No. NAS5-3953.

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ARACON PHOTOGRAMMETRIC ATTITUDE SYSTEM

HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

1. INTRODUCTION

Under Contract No. NAS5-3953, ARACON has developed a flexible photogrammetric satellite attitude determination system. Any satellite camera system which yields 35 mm film can be accommodated. System hardware is a general-purpose film reader along with formatting and control electronics (Fig. 1). Off-line operation of this equipment produces a paper tape filled with raw attitude data. Computer programs have been provided to calculate TIROS attitude parameters with the aid of a Control Data 160-A (with 8K memory and two tape transports). The system was first made operational for the TIROS IX wheel configuration satellite. Since then minor software changes have been made to accommodate TIROS X with its "conventional" camera mount geometry.

The paper tape produced by film reader operation contains several varieties of data, some numerical and some not. The primary numerical data are X-Y coordinates of three different types of data "points": landmarks, horizon points, and matchpoints (common features in pictures with overlapping coverage). These data are obtained by reading the positions of cursors centered by an operator over selected image points of cloud pictures displayed on the film reader.

Figure 2 shows the data displayed on the film reader screen. Two consecutive frames of TIROS 35 mm film appear on the right hand side of the screen. The upper frame can be rotated 360° by an operator to permit rotational alignment of the two TIROS frames, thereby facilitating matchpoint measurements. The legend of the lower frame is displayed immediately below the frame itself. Landmark maps, on a series of 35 mm slides, are displayed on the left-hand side of the screen.

Two sets of perpendicular crosswires (cursors) ride immediately behind the reader display screen. The intersection of each set defines a point in the image plane of the reader. Either set can be positioned at any point on the display screen. The projection mechanism and crosswire assemblies (not including the electronic readout) are described in detail in the "Itek - ARACON Film Record Reader" instruction manual, which accompanies and is considered to be part of this manual.

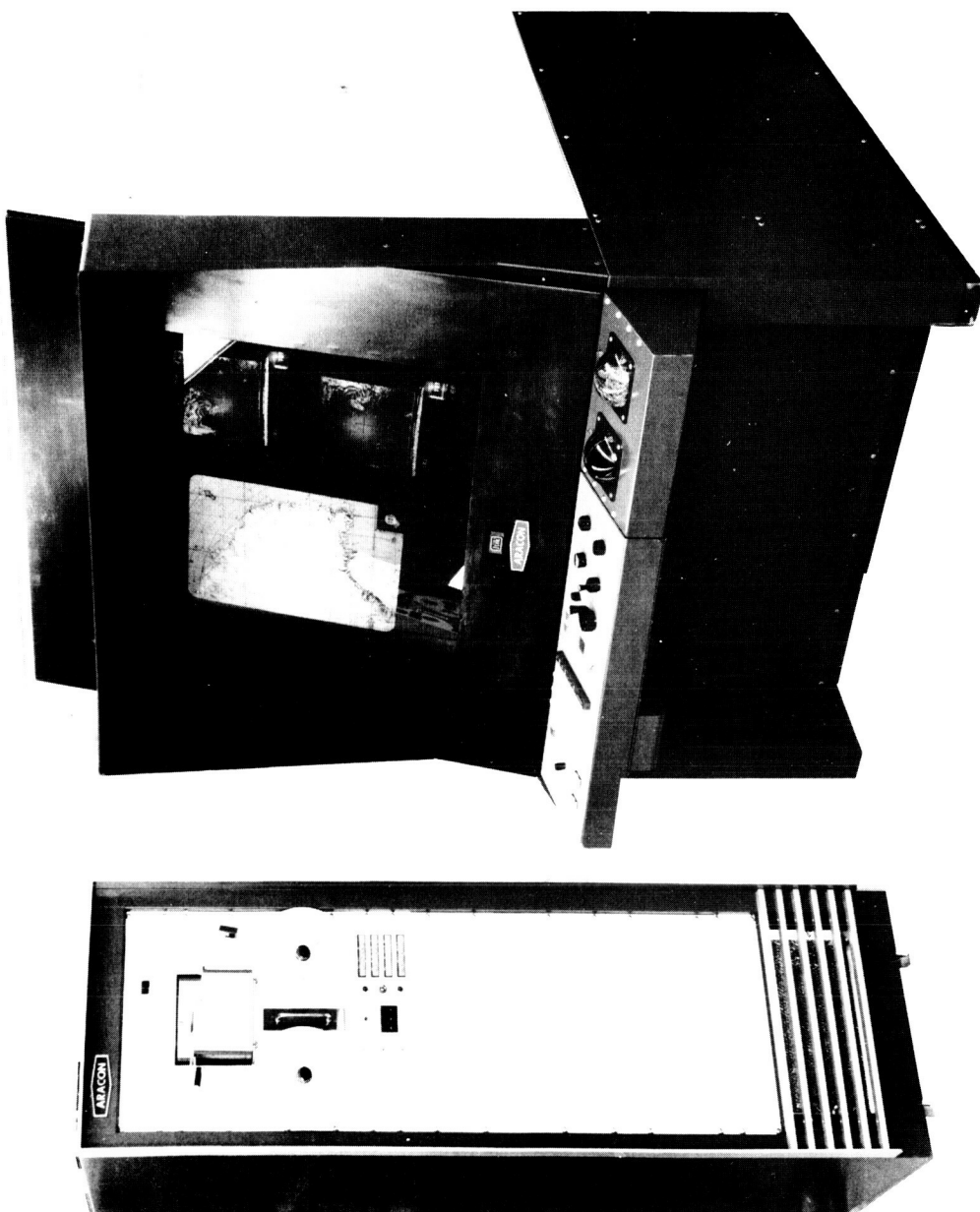


Fig. 1 Photogrammetric Attitude System

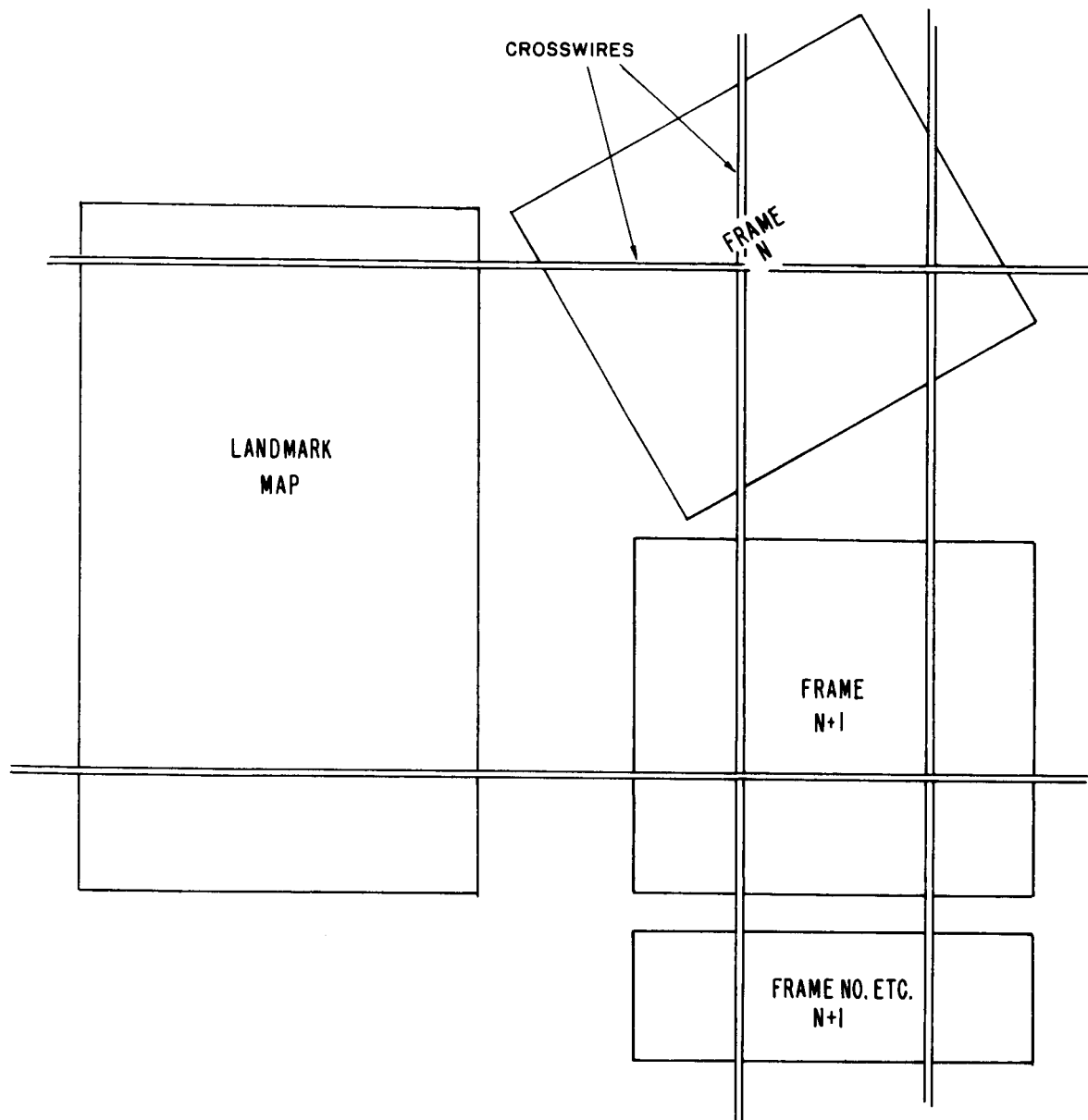


Fig. 2 Film Reader Display

Figure 3 shows a simplified block diagram of the electronics which convert crosswire position to digital codes punched on paper tape. A shaft position encoder is mechanically linked to the prism mechanism which rotates the upper TIROS image, providing an indication of image rotation. Additional data sources are a keyboard and control switches mounted on the control panel of the film reader. Data from the shaft encoders and the control panel are punched onto paper tape through an electronic sequencer.

A feature of the system is programmed control of the sequence of measurements to be made on each cloud picture. The type of point (picture fiducial, landmark, horizon point, etc.) defines the measurement "mode" of the reader. The mode is displayed to an operator from an illuminated display device mounted on the reader control panel. The order of measurement modes is determined by the pin setting of the mode sequence patchboard. After completing operations in a given mode, an operator depresses a mode advance pushbutton. The mode, or type of measurement, is also sequenced onto paper tape with the outputs of the shaft encoders.

A second patchboard allows selection of the various data sources for each type of measurement or mode. Each mode requires somewhat different data to be punched on tape. For instance, when measuring horizon points, data is taken from only the upper picture and the outputs of shaft encoders for only one crosswire set are needed, whereas matchpoint measurements require readout of both crosswire sets. The patchboard permits selection of the punched data for each of eight types of measurements or modes.

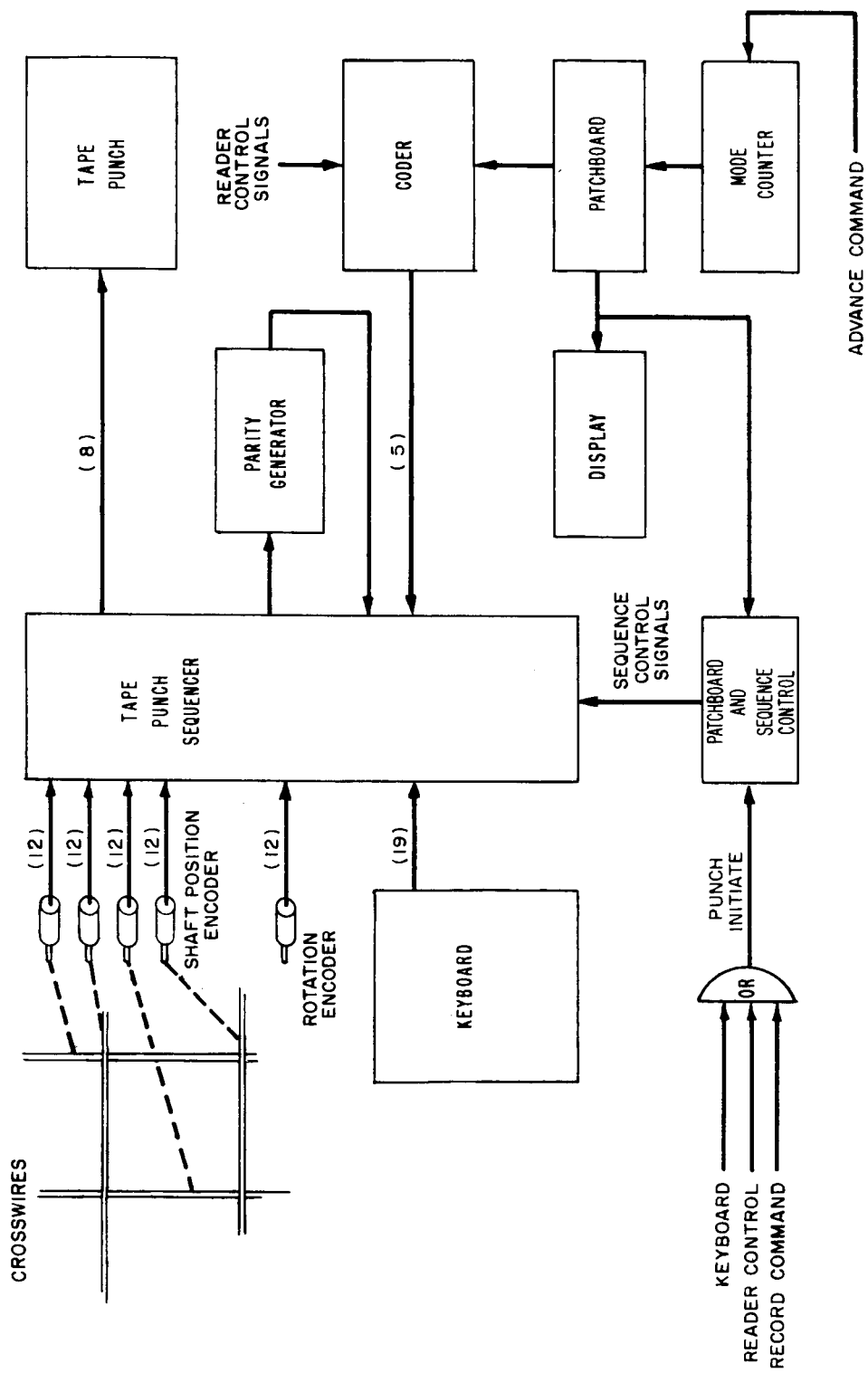


Fig. 3 Simplified System Block Diagram
Automated Attitude System

2. ORGANIZATION OF THE DATA

Two types of the punch records are applied to the 8-level paper tape. The first is a single-frame record used to record status or reader control signals. The second type consists of a number of frames, up to a maximum of fifteen, called mode records. A mode record always contains x, y information corresponding to one of the eight types of measurement or modes. Single frame punches always have a "ONE" in the highest two levels (2^7 , 2^6) of the frame.

Table 1 Punch Record Identification

	2^7						2^0
	Single Frame Punch						
	1	1	X	X	X	X	X
	Mode Record						
First Frame	1	0	X	X	X	X	X
	0	0	X	X	X	X	X
	0	0	X	X	X	X	X
	-	-	-	-	-	-	-
Last Frame	0	1	X	X	X	X	X

A mode record is identified by 1,0 for 2^7 and 2^6 of its first frame, 0,0 for interior frames of the record and 0,1 for the last frame. The lower six bits of the last frame of a mode record are used for longitudinal parity.

2.1 Single Frame Records

Table 2 is a list of the single frame records which can be punched on tape.

Table 2 Single Frame Records

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
NO READ UPPER	1	1	0	1	0	0	0	0
NO READ LOWER	1	1	0	1	0	0	0	1
START	1	1	1	1	0	0	0	0
ERASE	1	1	1	1	0	0	0	1
END	1	1	1	1	0	0	1	0
A	1	1	1	1	0	0	1	1
B	1	1	1	1	0	1	0	0
FILM FORWARD	1	1	1	0	0	0	0	0
FILM REVERSE	1	1	1	0	0	0	0	1
DECIMAL NUMBERS	1	1	0	0	X	X	X	X

[8, 4, 2, 1 BCD]

Each of the records (except the decimal numbers) listed in the above table is punched when an operator depresses the corresponding pushbutton switch on the film reader control panel shown in Figure 4. These records are essentially status instructions which are inspected by the computer for internal organization of the data. Their use is described in the Operator's Manual. A decimal number is punched into tape by (a) depressing the appropriate decimal switch in bank 2C(Fig. 4) and (b) depressing the Enter switch 3G. Decimal numbers are punched with the Enter switch, one at a time, using only the right hand bank of the keyboard.

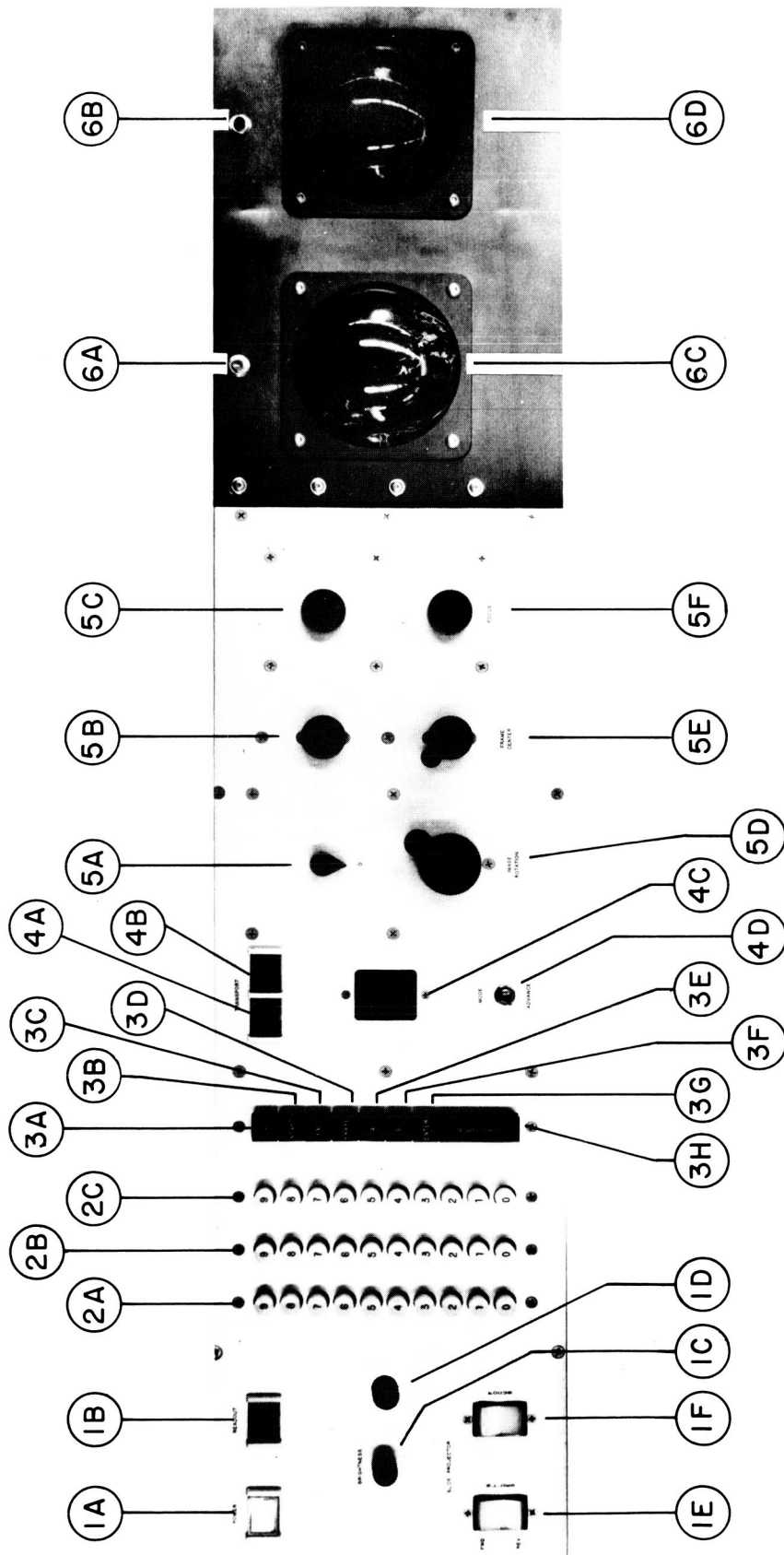
2.2 Mode Sequence

The type of measurement (mode) to be made by the operator appears in the window of the film reader control panel display (4C in Fig. 4). Eight modes are provided. These are:

Calibrate
Picture Fiducial

Fig. 4 Film Reader Control Panel

- | | | | | | |
|----|---|----|---|----|--|
| 1A | Main power switch (ON-OFF, Lightup) for film reader, logic rack and punch | 2C | Decimal keyboard, units digit (lightup) | 4D | Mode advance |
| 1B | ON-OFF switch (lightup) for logic rack and punch | 3A | Calibrate mode | 5A | Upper-picture gross rotation indicator |
| 1C | Slide-projector dimmer (0-120 V.A.C., solid state) | 3B | Start | 5B | Vertical position control for upper and lower pictures |
| 1D | Film-transport dimmer (0-120 V.A.C., Variac) | 3C | End | 5C | Upper picture focus |
| 1E | Slide-projector forward-reverse control | 3D | Erase (a single record) | 5D | Upper picture rotator |
| 1F | Slide-projector focus control | 3E | A (picture time code) | 5E | Horizontal position control for upper and lower pictures |
| 2A | Decimal keyboard, hundreds digit (lightup) | 3F | B (picture time code) | 5F | Lower-picture focus |
| 2B | Decimal keyboard, tens digit (lightup) | 3G | Enter (decimal keyboard nos.) | 6A | "Ignore lower crosswire" |
| | | 3H | Record | 6B | "Ignore upper crosswire" |
| | | 4A | Film transport forward | 6C | Lower-crosswire ball control |
| | | 4B | Film transport reverse | 6D | Upper-crosswire ball control |
| | | 4C | Mode indicator (lightup) | | |



Horizon
Matchpoint
Catalog Landmark
Map Fiducial
Unlisted Landmark
Auxiliary

The mode is controlled by an eight-state (three-stage) counter through the mode sequence patchboard. The first state of the counter (000) bypasses the patchboard and always corresponds to Calibrate. The remaining seven states of the counter are programmed to correspond to the other modes through the patchboard. The mode sequence patchboard is shown on the left in Figure 5. A shorting pin is inserted at the intersection of the mode and the counter state desired. An operator, depressing the mode advance pushbutton (4D on Fig. 4), will cause the mode sequence counter to advance one state. Thus the patchboard permits the seven modes other than Calibrate to appear in any sequence he chooses.

Depressing the Start switch (3B, Fig.4), or the film transport FWD, REV switches (4A and 4B) will always cause the counter to advance to its second state (listed as number 1 on the patchboard) so that an operator is not required to advance the mode counter through all its states to return to the beginning of a sequence of measurement modes. Column 8 on the mode patchboard is not used.

The calibrate mode is entered by depressing the CAL switch (3A). Depressing this switch also serves to create paper tape leader.

Normally the map fiducial mode is assigned to a counter state which is one less than the state number for unlisted landmark. If the Slides Forward, Reverse rocker switch is depressed it will always cause the mode counter to go back one state. Thus if an operator is in the unlisted landmark state and he changes slides, he will find that the measurement mode is changed to map fiducial.

2.3 Mode Records

When an operator depresses the Record switch (3H on Fig.4C) a mode record is punched on paper tape. The content and number of the frames which are punched on tape for each mode record depend on: 1) the measurement mode appearing in the mode display, 2) the program set up on the frame sequence patchboard.

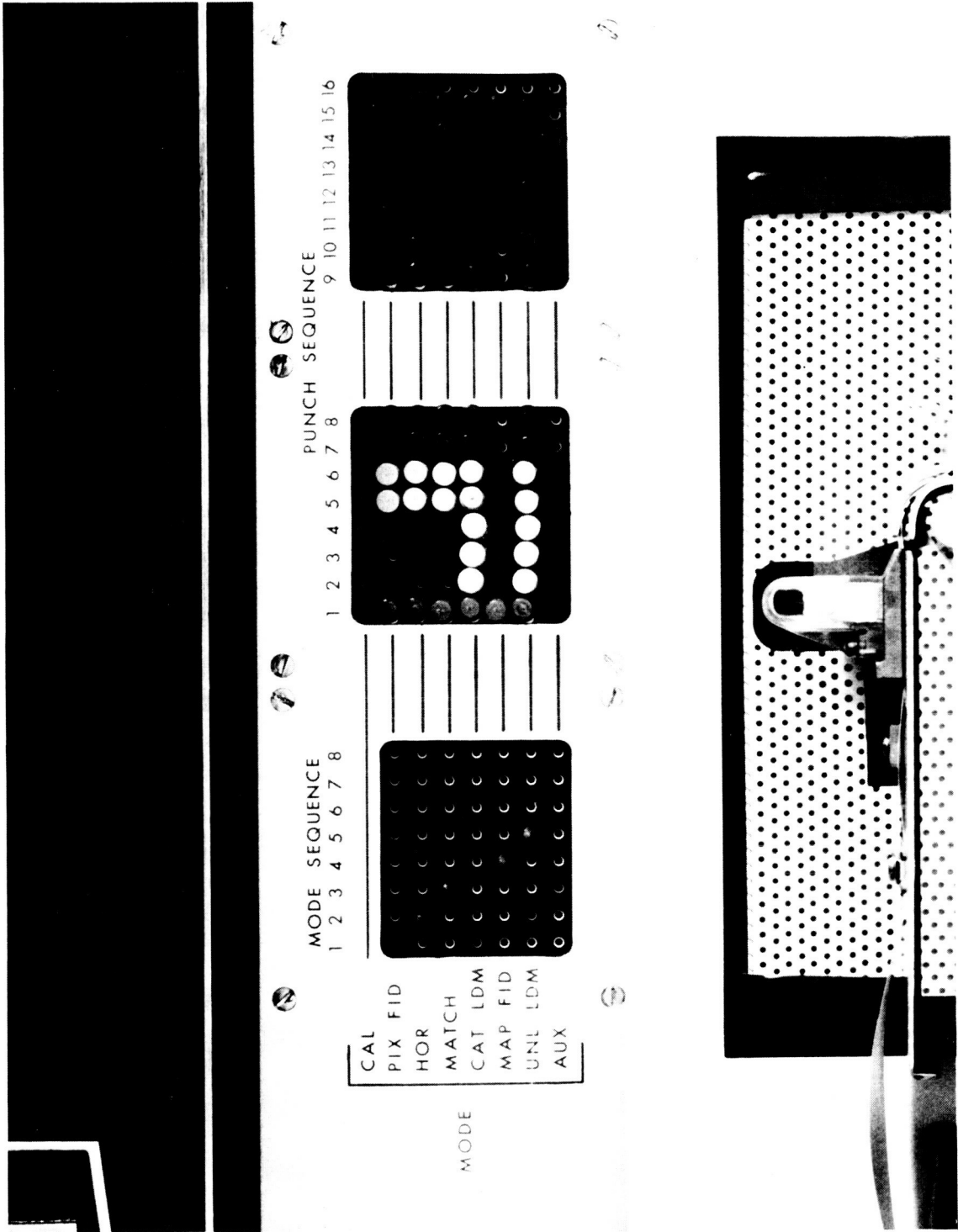


Fig. 5 Patchboard

The frame sequence patchboard is shown on the right-hand side of Figure 5. A mode record can contain as many as fifteen frames of data, depending on the patchboard programming. The content of these 15 possible frames is shown in Table 3.

When a number is assigned to a frame in this manual, it is always the number of the frame at the input gates of the sequencer, and not the number of the frame actually punched. The frames punched are determined by the presence of pins at the intersections of the mode and frame numbers on the patchboard.

KB1, KB2 and KB3 shown in Table 3 are 8421 binary-coded decimal characters from decimal keyboard banks 2A, 2B, and 2C (Fig.4) respectively.

The "upper" shaft encoders are those which are linked to the crosswires positioned by control 6C on the control panel. The "lower" encoders read the position of the crosswires driven by control 6D. Crosswires are labeled "upper" and "lower" to indicate that portion of the screen on which they are normally used.

The output of each encoder is a 12-bit gray code, with the upper and lower six bits comprising separate consecutive frames at the input of the sequencer.

The mode codes, which appear in frame 1 and serve to identify the type of measurement, are listed in Table 4. These codes emanate from a code generator whose inputs are the mode signals from the patchboard.

Table 3. Composition of Mode Records at Sequencer Input

Frame No.	Punch Level							
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0	X	X	X	X	X	X
			└─ Mode Code ─┘					
2	0	0	0	0	X	X	X	X
					└─ KB1 ─┘			
3	0	0	0	0	X	X	X	X
					└─ KB2 ─┘			
4	0	0	0	0	X	X	X	X
					└─ KB3 ─┘			
5	0	0	X	X	X	X	X	X
			└─ Rotation Encoder-Upper 6 Bits ─┘					
6	0	0	X	X	X	X	X	X
			└─ Rotation Encoder-Lower 6 Bits ─┘					
7	0	0	X	X	X	X	X	X
			└─ Upper X Encoder-Upper 6 Bits ─┘					
8	0	0	X	X	X	X	X	X
			└─ Upper X Encoder-Lower 6 Bits ─┘					
9	0	0	X	X	X	X	X	X
			└─ Upper Y Encoder-Upper 6 Bits ─┘					
10	0	0	X	X	X	X	X	X
			└─ Upper Y Encoder-Lower 6 Bits ─┘					
11	0	0	X	X	X	X	X	X
			└─ Lower X Encoder-Upper 6 Bits ─┘					
12	0	0	X	X	X	X	X	X
			└─ Lower X Encoder-Lower 6 Bits ─┘					
13	0	0	X	X	X	X	X	X
			└─ Lower Y Encoder-Upper 6 Bits ─┘					
14	0	0	X	X	X	X	X	X
			└─ Lower Y Encoder-Lower 6 Bits ─┘					
15	0	1	X	X	X	X	X	X
			└─ Even Logitudinal Parity ─┘					

Table 4. Table Modes

	2^5	2^4	2^3	2^2	2^1	2^0
Calibrate	0	0	0	0	0	0
Picture Fiducial	0	0	0	0	0	1
Horizon	0	0	0	0	1	0
Matchpoint	0	0	0	0	1	1
Catalog Landmark	0	0	0	1	0	0
Map Fiducial	0	0	0	1	0	1
Unlisted Landmark	0	0	0	1	1	0
Auxiliary	0	0	0	1	1	1

3. EQUIPMENT DESCRIPTION

A block diagram of the photogrammetric attitude system appears in Figure 6. The blocks contained within a rectangle defined by the dotted background are found on the drawing number (9G8-XXE) indicated in the rectangle. The numbers in parentheses indicate the number of signals passing between blocks. In some cases, a signal is actually transmitted by two leads for code and complement. However, it is indicated as a single signal on the block diagram. A glossary of abbreviations used for the various electrical signals in the block diagram and logic drawings appears in Table 5.

Figure 7 shows the system cabling and Figures 8 and 9 show connector and equipment locations.

The shaft position encoders are located in the film reader. The encoder outputs feed encoder registers located in the electronics rack. The register outputs in turn are fed to the frame gates which select the data to be punched on tape when the Record switch is depressed. A description of the encoders and encoders registers along with the wire lists for (1) cable connections between encoders and encoder registers and (2) connections between encoder register outputs and the frame gates, is found in Appendix A "Encoder Readout and Wiring."

The controls on the film reader are essentially divided into two assemblies; the keyboard, which includes the three banks of decimal switches and the adjacent bank CAL through RECORD, and the remainder of the switches distributed over the control panel. A schematic of the keyboard (Drawing No. 9G8-04E) is contained in Appendix B "Logic Diagrams and Wiring." The other control panel switches are shown in the electrical schematic of the ARACON Film Reader Manual. The control panel switches other than the keyboard, drive relays located in the top of the electronics rack. These relays convert the single throw action of the switches to a double throw action for input to the flip-flops of the switch-signal conditioners. The connections between the control panel and mode display of the film reader control panel are shown in the cable diagrams of Appendix B.

The logic and switching functions are accomplished with digital modules manufactured by Computer Control Company, Inc. These modules are located in three card cages mounted in the electronics rack and labeled A, B and C for top, middle and bottom respectively.

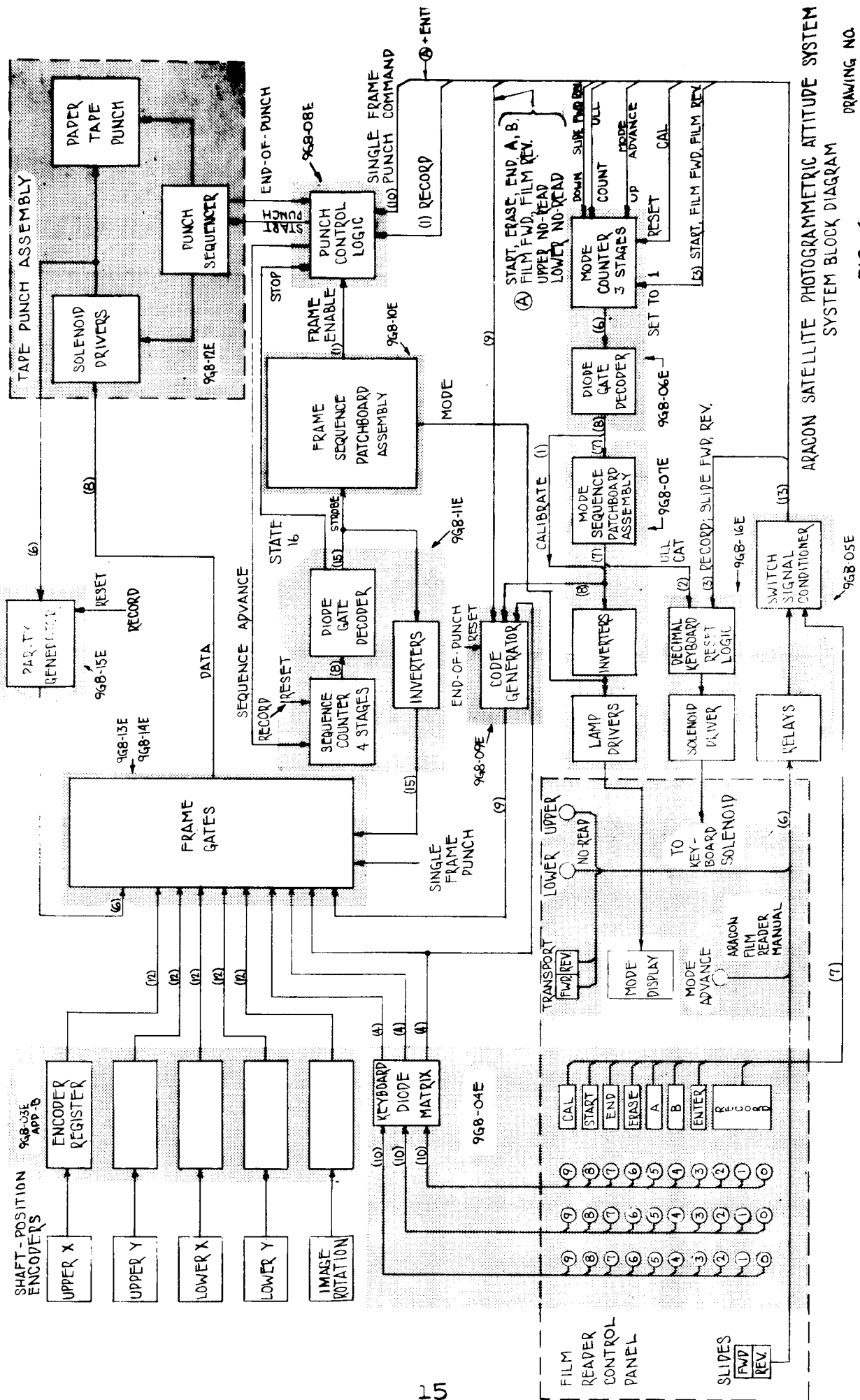


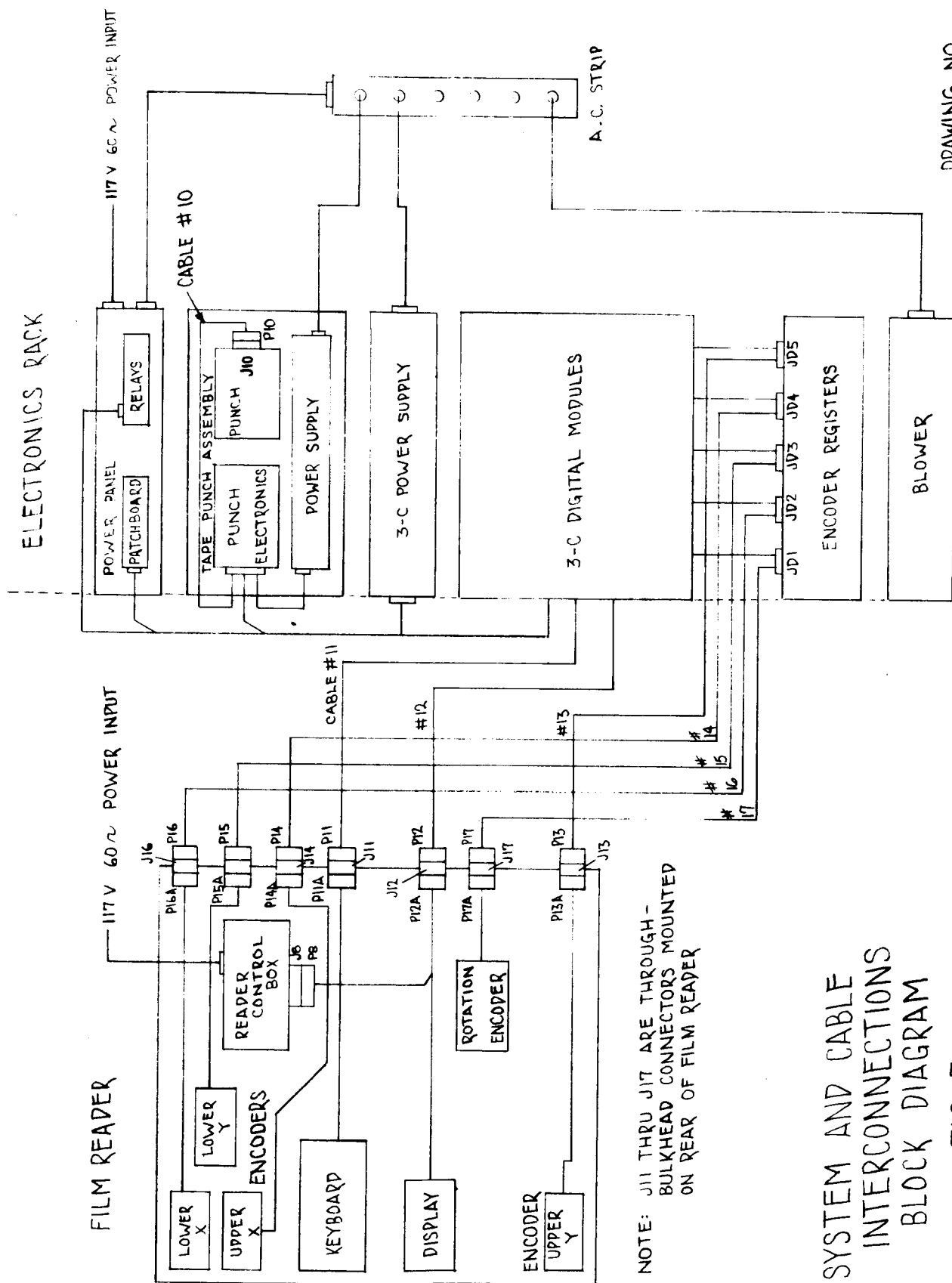
FIG. 6

ARACON SATELLITE PHOTOGRAMMETRIC ATTITUDE SYSTEM
SYSTEM BLOCK DIAGRAM

DRAWING NO.
968-01E

TABLE 5
LOGIC SIGNAL ABBREVIATIONS

ER	Erase
FREV	Film Reverse
FFWD	Film Forward
EM	End Message
SM	Start Message
REC	Record
LRND	Lower No Read
UPND	Upper No Read
KB 1	Keyboard Column 1
PO	Punch Output
PIX FID	Picture Fiducial
HOR	Horizon
AUX	Auxiliary
MAP FID	Map Fiducial
ULD	Unlisted Landmark
CAT	Catalog Landmark
MAT	Matchpoint
SEQ 1	Sequence 1
MS 1,2.....8	Mode and Sequence 1,2,.....8
SQ 2 ⁰2 ³	Sequence Counter Output
SEQ 1.....16	Sequence Timing
PT	Punch Trigger Pulse
MC	Mode Code
SPC	Single Punch Code



DRAWING NO.
9GB-02E

SYSTEM AND CABLE
INTERCONNECTIONS
BLOCK DIAGRAM
FIG 7

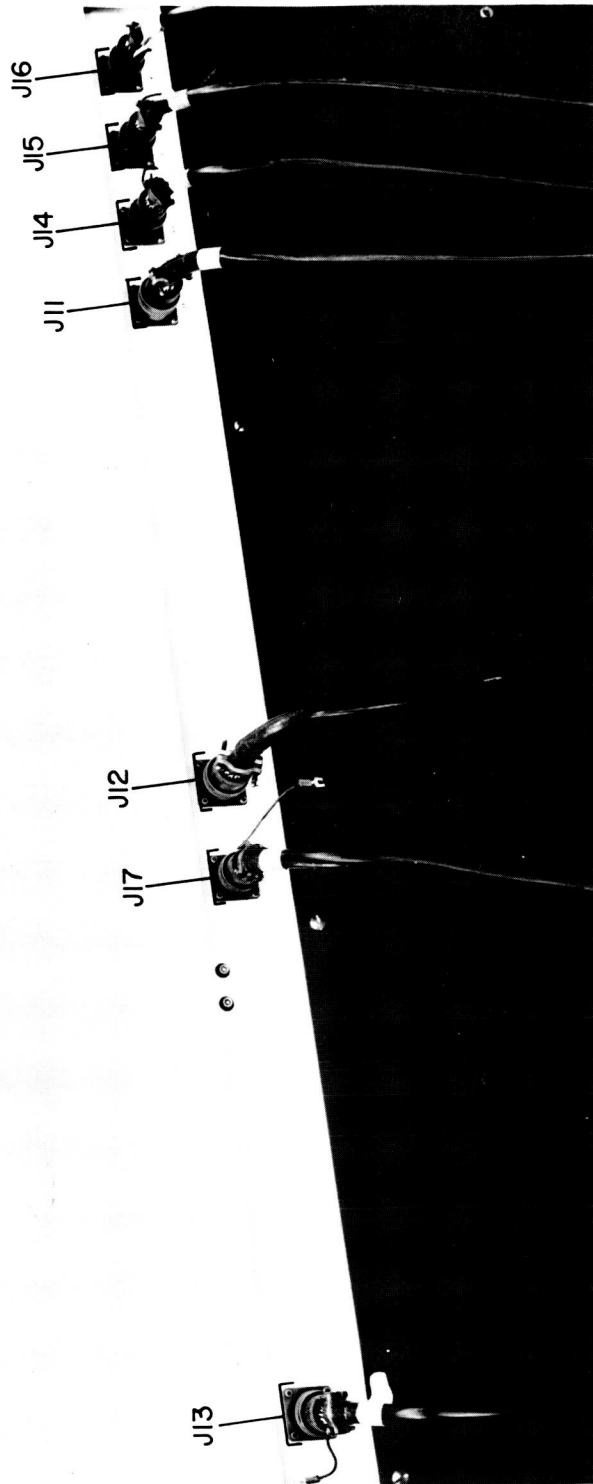


Fig. 8 Film Reader Connector Locations

The 3-stage mode counter and counter-state decoders are shown on Drawing 9G8-06E, Appendix B. A pulse derived from pushing the CAL switch, resets the mode counter to 000. The counter is advanced one state each time the Mode Advance switch is actuated. A signal from either the Start, Film Forward or Film Reverse switches sets the counter to state 2 (001) which is the first counter state delivered to the mode sequence patchboard. A Slide Forward or Slide Reverse signal decrements the mode counter if the counter is in the Unlisted Landmark mode. (This results in the counter reverting to the Map Fiducial mode if Map Fiducial is assigned to the counter state preceding Unlisted Landmark.) The outputs of the mode counter decoder (other than calibrate) are delivered to the mode patchboard (Drawing 9G8-07E) where the various states of the counter are assigned to measurement modes. The assigned mode corresponding to the counter state is displayed to an operator at the film reader control panel.

A punch is initiated by either the RECORD switch (for a mode record) or one of the other control panel switches (for a single frame punch). These signals are delivered to the punch control logic shown in Drawing 9G8-08E. A single frame punch command causes the output of the code generator (Drawing 9G8-09E) to be delivered by the frame gates to the type punch assembly simultaneously with a single Start-Punch command to the sequencer in the punch assembly. In this manner, outputs from the right hand bank of decimal switches and from the various control switches generate codes which are punched on the paper tape.

Mode records are initiated when the RECORD switch is depressed. This resets the sequence counter (Drawing No. 9G8-11E) causing the decoded output corresponding to first state of the counter to be fed to the frame sequence patchboard assembly (Drawing No. 9G8-10E). If a pin is inserted in the patchboard at the intersection of the mode and frame 1, a frame enable signal is delivered to the punch control logic which permits the delayed RECORD signal to generate a start-punch command. If the pin is absent, the delayed RECORD signal advances the sequence counter. After a frame is punched, an end-of-punch signal from the punch assembly advances the sequence counter to its next state. A delayed sequence advance signal either (1) sends another start punch signal to the punch assembly if a frame enable signal is present from the patchboard, or (2) advances the sequence counter if the frame enable is missing. This action is repeated until state 16 of the sequence counter is reached. Counter state 16 inhibits the end-of-punch signal from

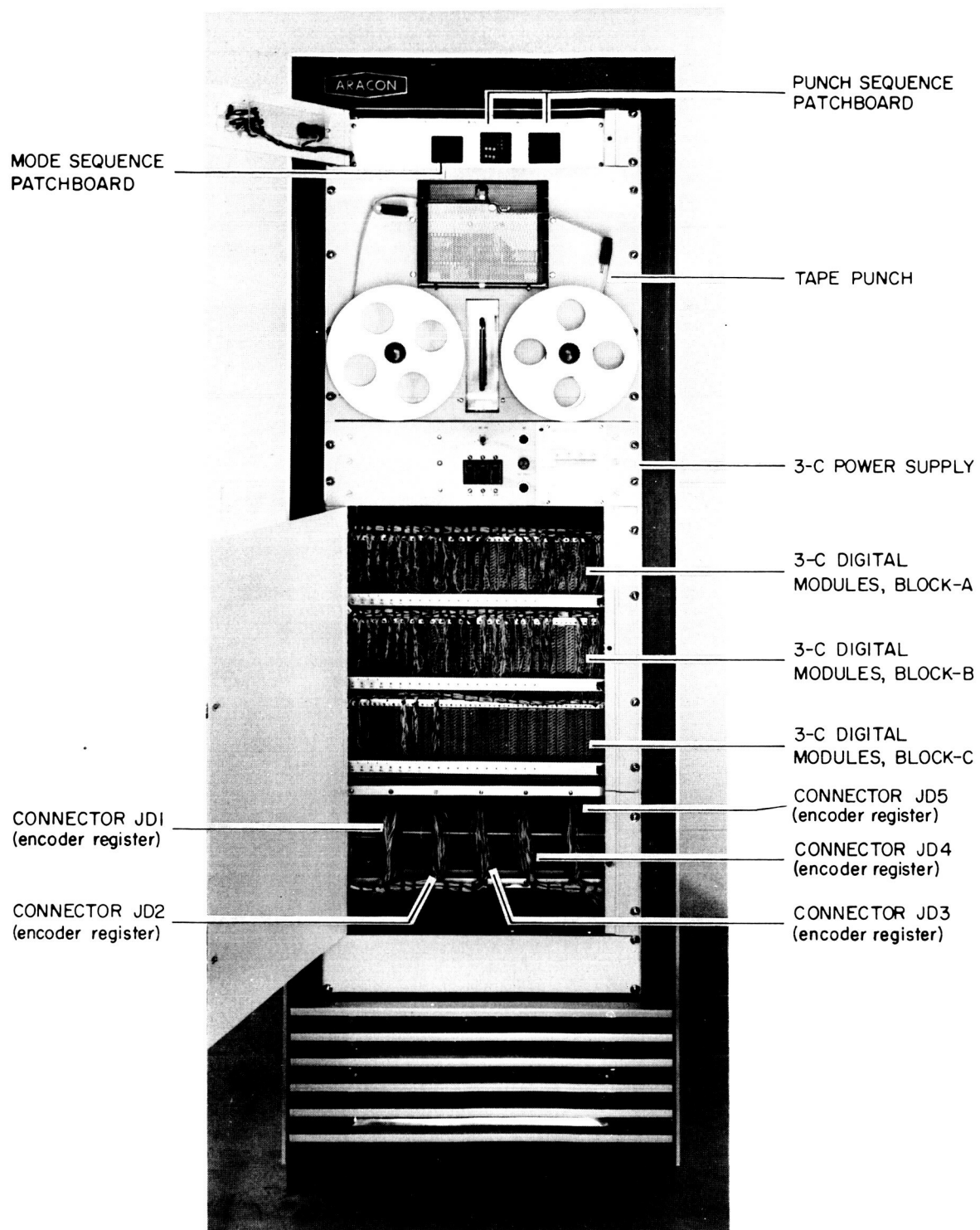


Fig. 9A Electronics Rack

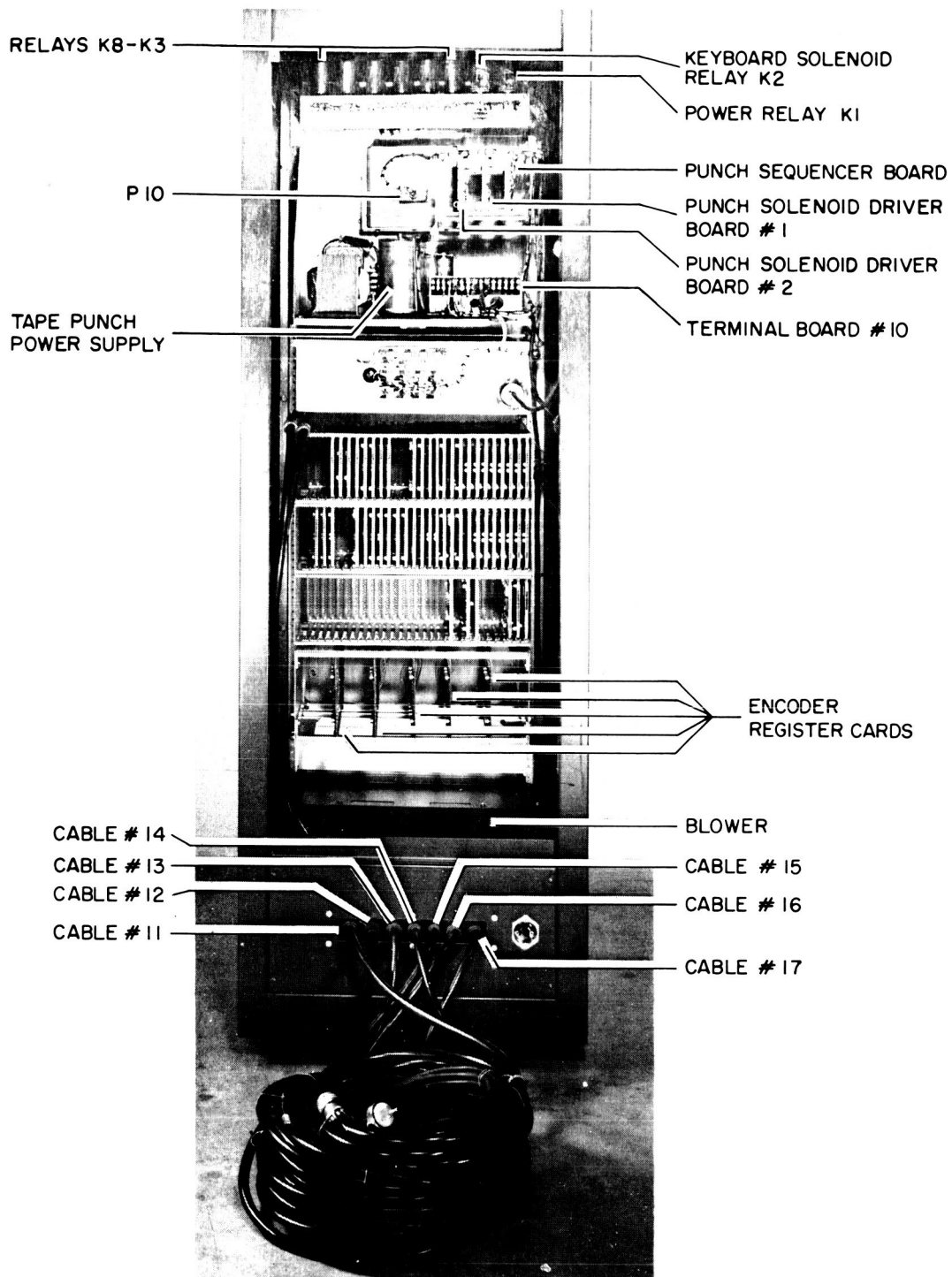


Fig. 9B Electronics Rack

the tape punch assembly, thereby completing the punch cycle. The frame gates (Drawings 9G8-13E and 9G8-14E) are enabled by the signals representing the counter states. Only that information corresponding to the frame represented by the state of the counter is punched when a frame enable is delivered from the patch-board to the punch control logic. The gates for frame 1 are fed by the code generator, the output of the code generator being determined by the system mode. The last (fifteenth) frame is the output of the parity generator flip-flops shown in Drawing 9G8-15E.

Drawing 9G8-12E shows the wiring of the punch solenoid drivers, punch sequencer, and tape punch. More detailed schematics of the punch assembly are available in the Invac tape punch manual. Drawing 9G8-17E is a schematic of the tape punch power supply.

The reset logic for the decimal keyboard is shown in Drawing 9G8-16E. In the catalog landmark mode, the keyboard is reset at the end of each mode record. In the unlisted landmark mode, the keyboard is reset only when a slide change occurs.

The power distribution for the electronics is shown in Drawing 9G8-18E. Power distribution for the film reader is shown in the electrical schematic of the ARACON Film Reader Manual.

The locations of the digital modules in the electronics rack are shown in Drawing 9G8-19E.

4. MAINTENANCE AND CALIBRATION

4.1 Preventive Maintenance

The only item in the electronic system requiring periodic maintenance is the paper tape punch. Every 90 days the punch should be inspected, cleaned and lubricated in accordance with the instructions in Section IV of the Tape Punch Instruction manual.

The filter in the blower assembly at the bottom of the electronics rack should be cleaned as required to ensure proper air flow.

The Perkin-Elmer shaft position encoders do not normally require maintenance. In the event of an encoder malfunction, the encoder should be replaced with a spare and the defective unit returned for repair.

Refer to Section 4 of "Itek-ARACON Film Record Reader" instruction manual for Film Reader maintenance.

4.2 System Checkout

The following system checkout procedure should be employed on approximately a bi-weekly basis, or when a system error is suspected.

1. Depress all switches which yield single-frame records and check the tape codes against those listed in Section 2.
2. Produce a frame record for each mode in use as determined from the patchboard program. Check high-level bits for correct first frame, interior frame, and last frame identification. Check mode code and parity frame. Count the number of frames per record and compare against patchboard program. Enter keyboard numbers on landmark modes and check for correct BCD code in frames 2, 3 and 4.
3. Insert reseau film strip in projector and position film so that the reseau grid is visible in the upper portion of the film-reader screen. Adjust frame position controls so that they are approximately in the middle of their control range. This produces minimum optical distortion. Insert pins in the Calibrate row of the frame sequence patchboard in frame positions 7, 8, 9 and 10 only. Measure the reseau grid coordinates using right-hand ball control, as follows:

4. a. depress CAL pushbutton, and then END pushbutton.
b. position crosswires over first intersection on grid. (The order of intersection measurement is left to the discretion of the operator). Depress Record pushbutton. Continue with successive grid intersections. When complete, again depress END pushbutton.
5. Position a reseau grid so that it appears in portion of screen reserved for the lower displayed image. Insert pins in CAL row of frame sequence patchboard in frame positions 11, 12, 13 and 14 only. Repeat 4 using left-hand ball control.
6. Convert gray code readings to decimal printout by using the gray code-to-decimal 160-A conversion routine. (See Appendix D). This yields a list of 4 digit decimal values, x before y, in the sequence in which they are punched on tape. Check the decimal values for the grid intersections. Make sure that increasing values of x and y are obtained in accordance with grid intersection position. Evaluate Δx and Δy between intersections on common lines. If differences in Δx or Δy in excess of 3 parts in 1000 are found, a realignment of the optical system is called for. See the Itek-ARACON Film Reader Manual for instructions.
7. If an encoder is suspect, the measurements on a grid may be repeated using a different crosswire set by shifting the pins in the patchboard from 7, 8, 9 and 10 to 11, 12, 13 and 14 or vice versa and also changing the ball control used for measurement.
8. Position a slide reseau grid in the slide projector and using CAL patchboard frames 11, 12, 13 and 14 and left hand ball control, repeat steps 4 through 7.
9. Record the x, y coordinates of the fiducial inscribed on the upper part of the screen using frames 7, 8, 9 and 10 only on sequence patchboard, using right hand ball for crosswire positioning. These values should be checked against those derived for the fiducial at the time of the most recent Image Rotation Calibration. (Image Rotation Calibration is described in the next section.) If the fiducial values are more than 1 count away from the Calibration values, a new Image Rotation Calibration should be performed. This completes system checkout.

4.3 Image Rotation Calibration

Certain parameters associated with the upper, rotatable image are entered in the programs which process the image data. These parameters are: (1) X ROTCT and Y ROTCT - the x, y coordinates, in shaft encoder counts, of the image-plane center of rotation at the screen; (2) NO ROT - the rotation encoder output for zero rotation (detented position of prism); and (3) PER 360 - the number of shaft encoder counts for 360° of image rotation.

X ROTCT, Y ROTCT

Project a reseau grid on upper part of display screen. Mentally pick a grid intersection near the center of the grid and watch it describe a circle as the image is rotated. Place the crosswires over the apparent center of rotation. Then use the image position controls (5B and 5E in Figure 4) to move the grid intersection previously tracked into coincidence with the crosswire intersection. Rotate the image again and repeat the above steps. When the grid and crosswire intersections remain coincident as the image is rotated, read out the x and y values by inserting pins in CAL row on sequence patchboard at frames 7, 8, 9 and 10, proceeding as described in Section 4.2, step 4. A more accurate estimate can be obtained by reading x, y values, for several degrees of rotation (45° , 90° , 135° 360°) of the corresponding points on the smallest circle (or ellipse) described by the selected grid intersection. Plot the x and y values separately against rotation and select the best average value of each for the computer program entry. Record the x, y values of the screen fiducial mark and keep a record of these numbers. If they change during subsequent calibration checks, new values for X NO ROTCT and Y NO ROTCT must be determined.

NO ROT

Place pins in frames 5 and 6 only of CAL row on sequence patchboard. Record output of shaft encoder. Rotate prism and return to detented position, again recording the encoder output. Do this several times and make sure the same value is repeated. Convert to decimal for entry to program.

PER 360°

Align a reseau grid line with the horizontal (or vertical) crosswire (patchboard setup same as for NO ROT) and record output. Rotate the image 360° and

align the same grid line with the same crosswire again. Record output. Do this several times. Convert values to decimal. Subtract low average value from high average value for entry to computer program.

APPENDIX A

ENCODER READOUT AND WIRING

The shaft-position encoders employed within the film reader are 8-turn, 1024 counts per turn units manufactured by Perkin-Elmer. The Perkin-Elmer ONE BRUSH shaft encoder employs a new concept in encoding absolute positional information which requires the encoder to transmit only the changes in positional information. The encoder "sets" and "resets" flip-flops in a register which stores the positional information. The encoder is merely required to command the memory flip-flops (rather than continuously generate the coded output as in conventional encoders).

The code disc consists of a flush, multilayer, printed circuit with pie-shaped commutator segments in the wiping path. A number of circular command conductors are located in several of the layers below the surface of the disc. Layers containing these command conductors are insulated from one another. Vertical connections between the code sectors and the command conductors are made by interconnecting pads located in the various layers. These pads are located so that a given commutator section is connected to one and only one command conductor.

The interconnection pattern between the commutator sectors and the command conductors is unique for each sector of the encoder, and forms the basis for generating absolute positional information. Thus, as the wiper moves over the commutator sectors, the command conductors are energized in a unique predetermined sequence. Tables A1 and A2 list the sequence for 1024 count/turn disc and Table A3 lists the command sequence for 8 count/turn disc. It is the voltages connected to the command conductors in the proper sequence which are used to set and reset the register flip-flops.

Table A-1
1024 COUNT ENCODER
COMMAND SEQUENCE

Bar No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	15	1	2	5	3	2	1	3	4	1	2	4	11	2	1	9
16	10	1	2	15	4	2	1	4	3	1	2	3	11	2	1	5
32	6	1	2	15	3	2	1	3	4	1	2	4	11	2	1	10
48	9	1	2	15	4	2	1	4	3	1	2	3	11	2	1	6
64	8	1	2	15	3	2	1	3	4	1	2	4	11	2	1	9
80	10	1	2	15	4	2	1	4	3	1	2	3	11	2	1	8
96	7	1	2	15	3	2	1	3	4	1	2	4	11	2	1	10
112	9	1	2	15	4	2	1	4	3	1	2	3	7	2	1	11
128	12	1	2	7	3	2	1	3	4	1	2	4	15	2	1	9
144	10	1	2	15	4	2	1	4	3	1	2	3	12	2	1	7
160	8	1	2	15	3	2	1	3	4	1	2	4	12	2	1	10
176	9	1	2	15	4	2	1	4	3	1	2	3	12	2	1	8
192	6	1	2	15	3	2	1	3	4	1	2	4	12	2	1	9
208	10	1	2	15	4	2	1	4	3	1	2	3	12	2	1	6
224	5	1	2	15	3	2	1	3	4	1	2	4	12	2	1	10
240	9	1	2	15	4	2	1	4	3	1	2	3	5	2	1	12

Table A-1 (continued)

Bar No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
256	14	1	2	5	3	2	1	3	4	1	2	4	15	2	1	9
272	10	1	2	15	4	2	1	4	3	1	2	3	14	2	1	5
288	6	1	2	15	3	2	1	3	4	1	2	4	14	2	1	10
304	9	1	2	15	4	2	1	4	3	1	2	3	14	2	1	6
320	8	1	2	15	3	2	1	3	4	1	2	4	14	2	1	9
336	10	1	2	15	4	2	1	4	3	1	2	3	14	2	1	8
352	7	1	2	15	3	2	1	3	4	1	2	4	14	2	1	10
368	9	1	2	15	4	2	1	4	3	1	2	3	7	2	1	14
384	13	1	2	7	3	2	1	2	3	1	2	4	15	2	1	9
400	10	1	2	15	4	2	1	4	3	1	2	3	13	2	1	7
416	8	1	2	15	3	2	1	3	4	1	2	4	13	2	1	10
432	9	1	2	15	4	2	1	4	3	1	2	3	13	2	1	8
448	6	1	2	15	3	2	1	3	4	1	2	4	13	2	1	9
464	10	1	2	15	4	2	1	4	3	1	2	3	13	2	1	6
480	5	1	2	15	3	2	1	3	4	1	2	4	13	2	1	10
496	9	1	2	13	4	2	1	4	3	1	2	3	5	2	1	15

Table A-1 (continued)

Bar No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
512	16	1	2	5	3	2	1	3	4	1	2	4	13	2	1	9
528	10	1	2	16	4	2	1	4	3	1	2	3	13	2	1	5
544	6	1	2	16	3	2	1	3	4	1	2	4	13	2	1	10
560	9	1	2	16	4	2	1	4	3	1	2	3	13	2	1	6
567	8	1	2	16	3	2	1	3	4	1	2	4	13	2	1	9
592	10	1	2	16	4	2	1	4	3	1	2	3	13	2	1	8
608	7	1	2	16	3	2	1	3	4	1	2	4	13	2	1	10
624	9	1	2	16	4	2	1	4	3	1	2	3	7	2	1	13
640	14	1	2	7	3	2	1	3	4	1	2	4	16	2	1	9
656	10	1	2	16	4	2	1	4	3	1	2	3	14	2	1	7
672	8	1	2	16	3	2	1	3	4	1	2	4	14	2	1	10
688	9	1	2	16	4	2	1	4	3	1	2	3	14	2	1	8
704	6	1	2	16	3	2	1	3	4	1	2	4	14	2	1	9
720	10	1	2	16	4	2	1	4	3	1	2	3	14	2	1	6
736	5	1	2	16	3	2	1	3	4	1	2	4	14	2	1	10
752	9	1	2	16	4	2	1	4	3	1	2	3	5	2	1	14

Table A-1 (continued)

Bar No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
768	12	1	2	5	3	2	1	3	4	1	2	4	16	2	1	9
784	10	1	2	16	4	2	1	4	3	1	2	3	12	2	1	5
800	6	1	2	16	3	2	1	3	4	1	2	4	12	2	1	10
816	9	1	2	16	4	2	1	4	3	1	2	3	12	2	1	6
832	8	1	2	16	3	2	1	3	4	1	2	4	12	2	1	9
848	10	1	2	16	4	2	1	4	3	1	2	3	12	2	1	8
864	7	1	2	16	3	2	1	3	4	1	2	4	12	2	1	10
880	9	1	2	16	4	2	1	4	3	1	2	3	7	2	1	12
896	11	1	2	7	3	2	1	3	4	1	2	4	16	2	1	9
912	10	1	2	16	4	2	1	4	3	1	2	3	11	2	1	7
928	8	1	2	16	3	2	1	3	4	1	2	4	11	2	1	10
944	9	1	2	16	4	2	1	4	3	1	2	3	11	2	1	8
960	6	1	2	16	3	2	1	3	4	1	2	4	11	2	1	9
976	10	1	2	16	4	2	1	4	3	1	2	3	11	2	1	6
992	5	1	2	16	3	2	1	3	4	1	2	4	11	2	1	10
1008	9	1	2	11	4	2	1	4	3	1	2	3	5	2	1	16

Table A-2

COMMAND DEFINITIONS
1024 Count Encoder

<u>Command Number</u>	<u>Function</u>	<u>Command Number</u>	<u>Function</u>
0	$\overline{A} \overline{C}$	9	\overline{E}
1	$A \overline{B}$	10	E
2	A B	11	$\overline{H} \overline{I}$
3	$\overline{A} C \overline{D}$	12	$H \overline{I}$
4	$\overline{A} C D$	13	$\overline{H} I$
5	$\overline{F} \overline{G}$	14	H I
6	$F \overline{G}$	15	\overline{J}
7	$\overline{F} G$	16	J
8	F G		

Commands 5 through 16 are "OR'd" to create Command Number 0

Indexing interval = 31 counts (worst case)

Example - $\overline{A} \overline{C}$: Flip-flops "A" and "C" commanded to "Reset" state

A B: Flip-flops "A" and "B" commanded to "Set" state.

TABLE A-3

8 COUNT COMMUTATOR DISC
COMMAND SEQUENCE

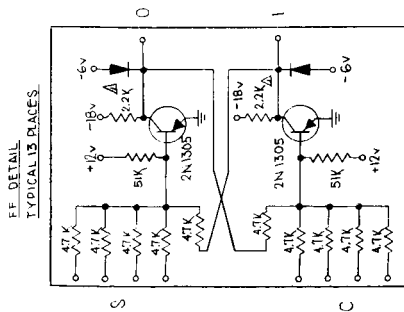
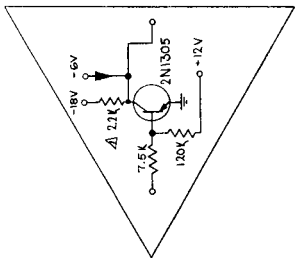
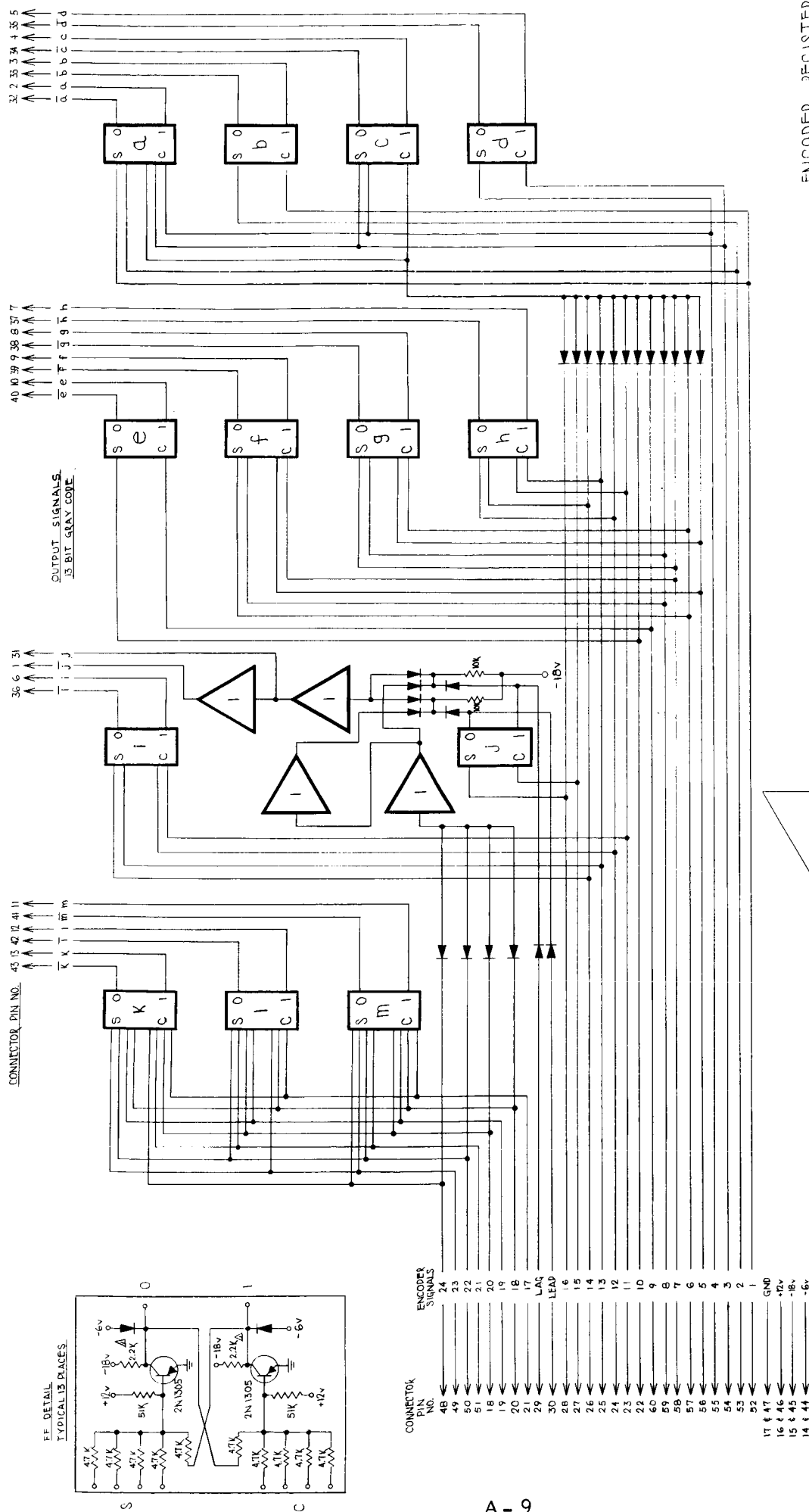
<u>Bar No.</u>	<u>Command No.</u>	<u>Command Definition</u>
0	17	$\bar{K} \bar{L} \bar{M}$
1	18	$K \bar{L} \bar{M}$
2	19	$K L \bar{M}$
3	20	$\bar{K} L \bar{M}$
4	21	$\bar{K} L M$
5	22	$K L M$
6	23	$K \bar{L} M$
7	24	$\bar{K} \bar{L} M$

Encoder Register

The encoder register is assembled from a number of flip-flops which are set or reset by a signal appearing on the command leads. A simplified schematic of the register is shown in Fig. A1. The functional blocks contained in the diagram used throughout this section to describe the encoder/register operation are composed of standard circuits.

The operation of the register flip-flops is as follows. When a -6 volt input (logical "one") appears on a command lead, it causes the transistors which are connected to the lead to fully conduct. Since only one command lead is energized at one time, it follows that the remaining transistors in the register will either remain in their previous state, or assume an off state because the opposite element of the flip-flop has been turned on. Obviously, transistors already on will not be affected by a one on their command lead. Since the feedback to the transistors is positive, the flip-flop latches up and remains in the present state even if the command signal is removed. The flip-flop changes states only when another command signal so directs. Note that the register flip-flops have two inputs, an "S" for "set" and an "R" for "reset". The corresponding outputs are "1" and "0" (also called the "true" and "complemented" outputs). When a flip-flop is set, its true output is equal to logical "one" (-6 volts) and when it is reset, the true output is equal to logical "zero" (0 volt). The complemented output assumes the opposite voltage levels.

Table A4 lists the encoder gray code outputs. The wire lists for cables 13 through 17 (rear of Appendix A) list the connections of the encoder output leads, through the cables, to the encoder register connections pens. The column at the right hand side of the page lists the encoder command functions shown on the encoder register drawing, Figure A-1. Wire lists of the connections between the register outputs and the digital-module, frame-gate inputs are also contained in the rear of this appendix.



Tabel A-4

Encoder Outputs

Logic Level

Binary 1 = -6V
 Binary 0 = 0 V
 Max Cur = 2 MA

<u>Gray Code Function</u>	<u>Connector Pin</u>
$\frac{A}{A}$	2 32
$\frac{B}{B}$	3 33
$\frac{C}{C}$	4 34
$\frac{D}{D}$	5 35
$\frac{E}{E}$	10 40
$\frac{F}{F}$	9 39
$\frac{G}{G}$	8 38
$\frac{H}{H}$	7 37
$\frac{I}{I}$	6 36
$\frac{J}{J}$	31 1
$\frac{K}{K}$	13 43
$\frac{L}{L}$	12 42
Common	17 and 47

Note: $\frac{L}{L}$ is most significant digit

WIRE LIST - CABLE #15

<u>Rack</u>	<u>J5</u>	<u>TB5</u>	<u>P5</u>	<u>Film Reader - Lower Y Shaft Encoder*</u>	
DJ3-52	A	A	A	Black	1
DJ3-53	B	B	B	Black-orange	2
DJ3-54	C	C	C	Black-yellow	3
DJ3-55	D	D	D	Black-green	4
DJ3-56	E	E	E	Black-blue	5
DJ3-57	F	F	F	Black-violet	6
DJ3-58	G	G	G	Black-gray	7
DJ3-59	H	H	H	Black-red	8
DJ3-60	J	J	J	Red-red	9
DJ3-22	K	K	K	Red	10
DJ3-23	L	L	L	Red-yellow	11
DJ3-24	M	M	M	Red-green	12
DJ3-25	N	N	N	Red-blue	13
DJ3-26	P	P	P	Red-violet	14
DJ3-27	R	R	R	Red-gray	15
DJ3-28	S	S	S	Red-orange	16
DJ3-21	T	T	T	Brown-black	17
DJ3-20	U	U	U	Brown-brown	18
DJ3-19	V	V	V	Brown-red	19
DJ3-18	W	W	W	Brown-orange	20
DJ3-51	X	X	X	Brown-yellow	21
DJ3-50	Y	Y	Y	Brown-green	22
DJ3-49	Z	Z	Z	Brown-blue	23
DJ3-14 and 44	a	a	a	Orange-blue	-6V.
DJ3-30	b	b	b	Orange-orange	Lead
DJ3-29	c	c	c	Orange-green	LAG
	No connection			Brown-violet	-6V.

* Sequencer input frames 13 and 14.

WIRE LIST - CABLE #16

<u>Rack</u>	<u>P16</u>	<u>J16</u>	<u>P16A</u>	<u>Film Reader - Lower X Shaft Encoder*</u>	
DJ2-52	A	A	A	Black	1
DJ2-53	B	B	B	Black-orange	2
DJ2-54	C	C	C	Black-yellow	3
DJ2-55	D	D	D	Black-green	4
DJ2-56	E	E	E	Black-blue	5
DJ2-57	F	F	F	Black-violet	6
DJ2-58	G	G	G	Black-gray	7
DJ2-59	H	H	H	Black-red	8
DJ2-60	J	J	J	Red-red	9
DJ2-22	K	K	K	Red	10
DJ2-23	L	L	L	Red-yellow	11
DJ2-24	M	M	M	Red-green	12
DJ2-25	N	N	N	Red-blue	13
DJ2-26	P	P	P	Red-violet	14
DJ2-27	R	R	R	Red-gray	15
DJ2-28	S	S	S	Red-orange	16
DJ2-21	T	T	T	Brown-black	17
DJ2-20	U	U	U	Brown-brown	18
DJ2-19	V	V	V	Brown-red	19
DJ2-18	W	W	W	Brown-orange	20
DJ2-51	X	X	X	Brown-yellow	21
DJ2-50	Y	Y	Y	Brown-green	22
DJ2-49	Z	Z	Z	Brown-blue	23
DJ2-14 and 44	a	a	a	Orange-blue	-6V.
DJ2-30	b	b	b	Orange-orange	Lead
DJ2-29	c	c	c	Orange-green	LAG
	No connection			Brown-violet	-6V.

* Sequencer input frames 11 and 12.

CABLE WIRE LIST - CABLE #17

<u>Rack</u>	<u>P17</u>	<u>J17</u>	<u>P14A</u>	<u>Film Reader - Rotary Encoder*</u>	
DJ1-52	A	A	A	Black	1
DJ1-53	B	B	B	Black-orange	2
DJ1-54	C	C	C	Black-yellow	3
DJ1-55	D	D	D	Black-green	4
DJ1-56	E	E	E	Black-blue	5
DJ1-57	F	F	F	Black-violet	6
DJ1-58	G	G	G	Black-gray	7
DJ1-59	H	H	H	Black-red	8
DJ1-60	J	J	J	Red-red	9
DJ1-22	K	K	K	Red	10
DJ1-23	L	L	L	Red-yellow	11
DJ1-24	M	M	M	Red-green	12
DJ1-25	N	N	N	Red-blue	13
DJ1-26	P	P	P	Red-violet	14
DJ1-27	R	R	R	Red-gray	15
DJ1-28	S	S	S	Red-orange	16
DJ1-21	T	T	T	Brown-black	17
DJ1-20	U	U	U	Brown-brown	18
DJ1-19	V	V	V	Brown-red	19
DJ1-18	W	W	W	Brown-orange	20
DJ1-51	X	X	X	Brown-yellow	21
DJ1-50	Y	Y	Y	Brown-green	22
DJ1-49	Z	Z	Z	Brown-blue	23
DJ1-14 and 44	a	a	a	Orange-blue	-6V.
DJ1-30	b	b	b	Orange-orange	Lead
DJ1-29	c	c	c	Orange-green	LAG
	No connection			Brown-violet	24

* Sequencer input frames 5 and 6.

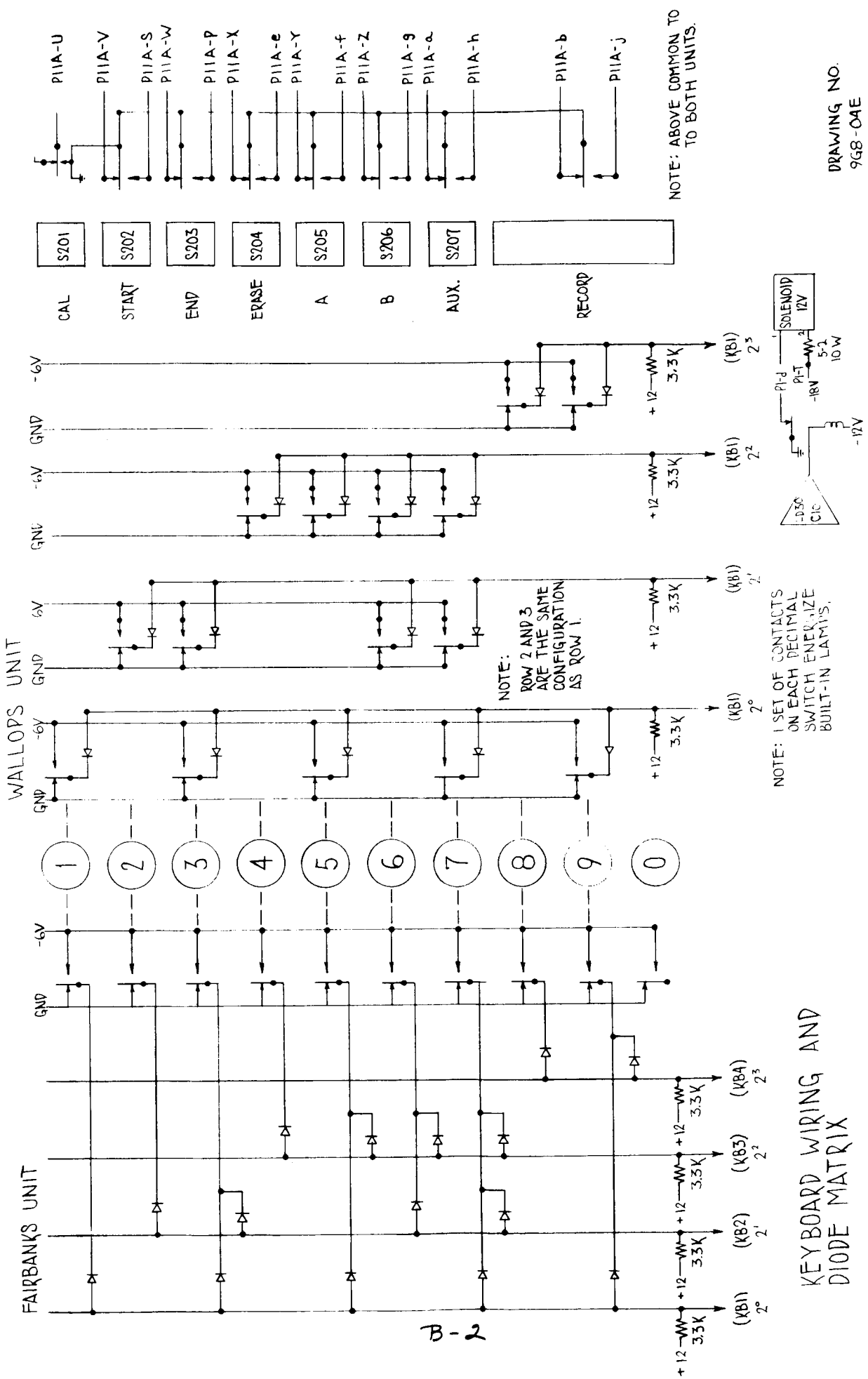
WIRE LIST - ENCODER REGISTER OUTPUTS

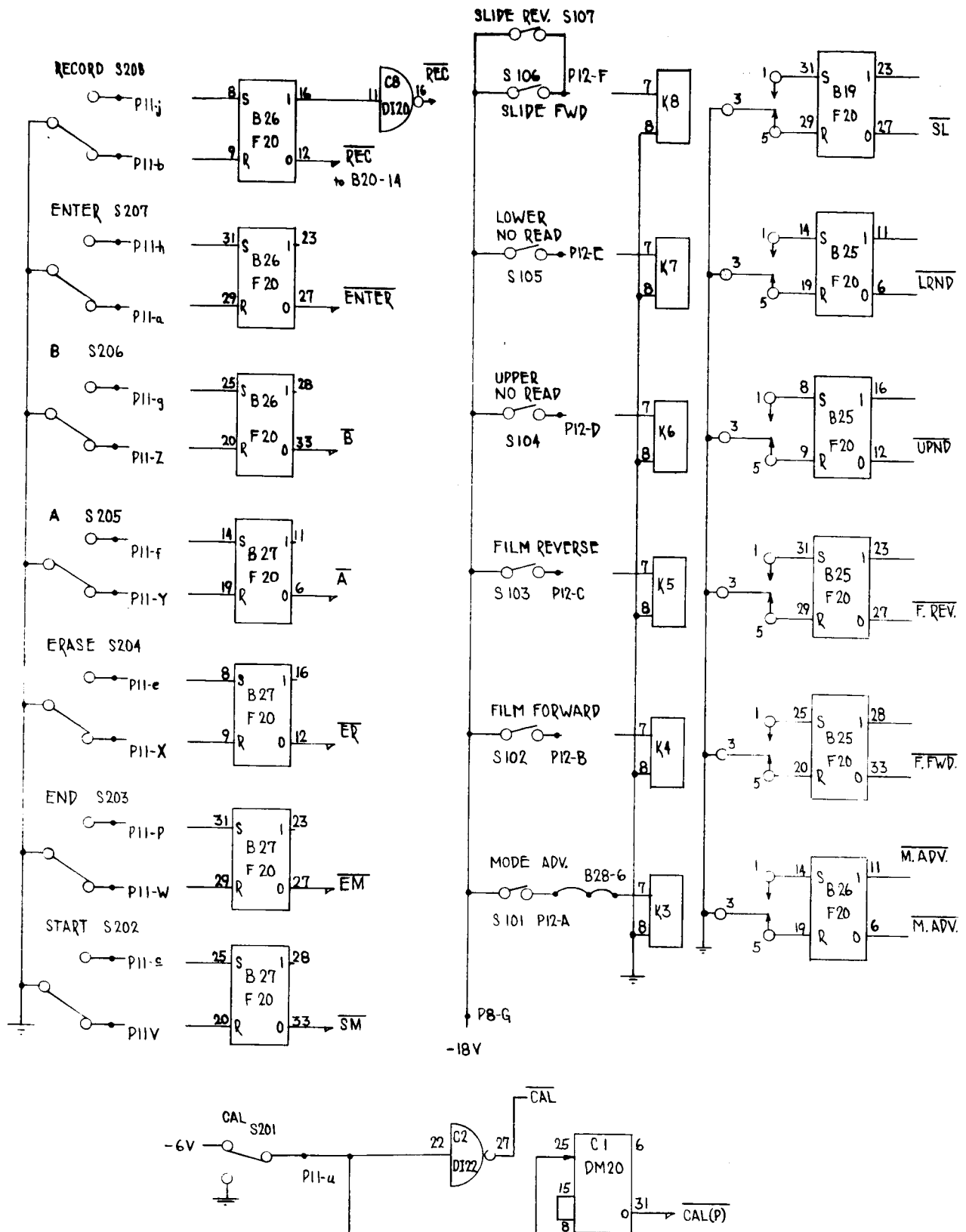
	<u>Sequencer Input Signal</u>	<u>Encoder Register Connector Pin No.</u>	<u>3-C Module Pin No.</u>
Frame #6, Rotation Encoder	2^0	DJ1-2	A1-26
	2^1	DJ1-3	A4-19
	2^2	DJ1-4	A7-9
	2^3	DJ1-5	B1-26
	2^4	DJ1-10	B3-31
	2^5	DJ1-9	B6-9
Frame #5, Rotation Encoder	2^0	DJ1-8	A1-31
	2^1	DJ1-7	A4-21
	2^2	DJ1-6	A7-14
	2^3	DJ1-31	B1-31
	2^4	DJ1-13	B4-9
	2^5	DJ1-12	B6-14
Frame #8, Upper X Encoder	2^0	DJ4-2	A2-9
	2^1	DJ4-3	A4-26
	2^2	DJ4-4	A7-19
	2^3	DJ4-5	B2-9
	2^4	DJ4-10	B4-14
	2^5	DJ4-9	B6-19
Frame #7, Upper X Encoder	2^0	DJ4-8	A2-14
	2^1	DJ4-7	A4-31
	2^2	DJ4-6	A7-21
	2^3	DJ4-31	B2-14
	2^4	DJ4-13	B4-19
	2^5	DJ4-12	B6-21

	<u>Sequencer Input Signal</u>	<u>Encoder Register Connector Pin No.</u>	<u>3-C Module Pin No.</u>
Frame #10, Upper Y Encoder	2^0	DJ5-2	A2-19
	2^1	DJ5-3	A5-9
	2^2	DJ5-4	A7-26
	2^3	DJ5-5	B2-19
	2^4	DJ5-10	B4-21
	2^5	DJ5-9	B6-26
Frame #9, Upper Y Encoder	2^0	DJ5-8	A2-21
	2^1	DJ5-7	A5-14
	2^2	DJ5-6	A7-31
	2^3	DJ5-31	B2-21
	2^4	DJ5-13	B4-26
	2^5	DJ5-12	B6-31
Frame #12, Lower X Encoder	2^0	DJ2-2	A2-26
	2^1	DJ2-3	A5-19
	2^2	DJ2-4	A8-9
	2^3	DJ2-5	B2-26
	2^4	DJ2-10	B4-31
	2^5	DJ2-9	B7-9
Frame #11, Lower X Encoder	2^0	DJ2-8	A2-31
	2^1	DJ2-7	A5-21
	2^2	DJ2-6	A8-14
	2^3	DJ2-31	B2-31
	2^4	DJ2-13	B5-9
	2^5	DJ2-12	B7-14
Frame #14, Lower Y Encoder	2^0	DJ3-2	A3-9
	2^1	DJ3-3	A5-26
	2^2	DJ3-4	A8-19
	2^3	DJ3-5	B3-9
	2^4	DJ3-10	B5-14
	2^5	DJ3-9	B7-19

	<u>Sequencer Input Signal</u>	<u>Encoder Register Connector Pin No.</u>	<u>3-C Module Pin No.</u>
Frame #13, Lower Y Encoder	2^0	DJ3-8	A3-14
	2^1	DJ3-7	A5-31
	2^2	DJ3-6	A8-21
	2^3	DJ3-31	B3-14
	2^4	DJ3-13	B5-19
	2^5	DJ3-12	B7-21

APPENDIX B
LOGIC DIAGRAMS AND WIRING

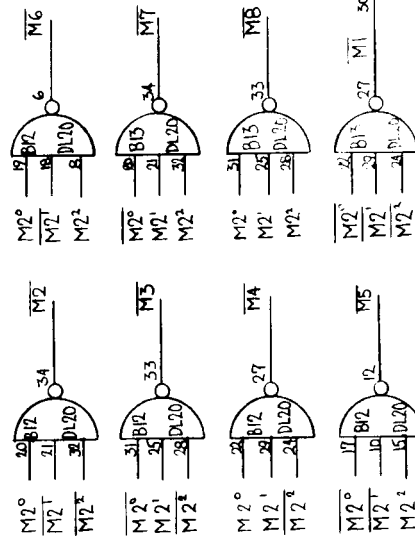
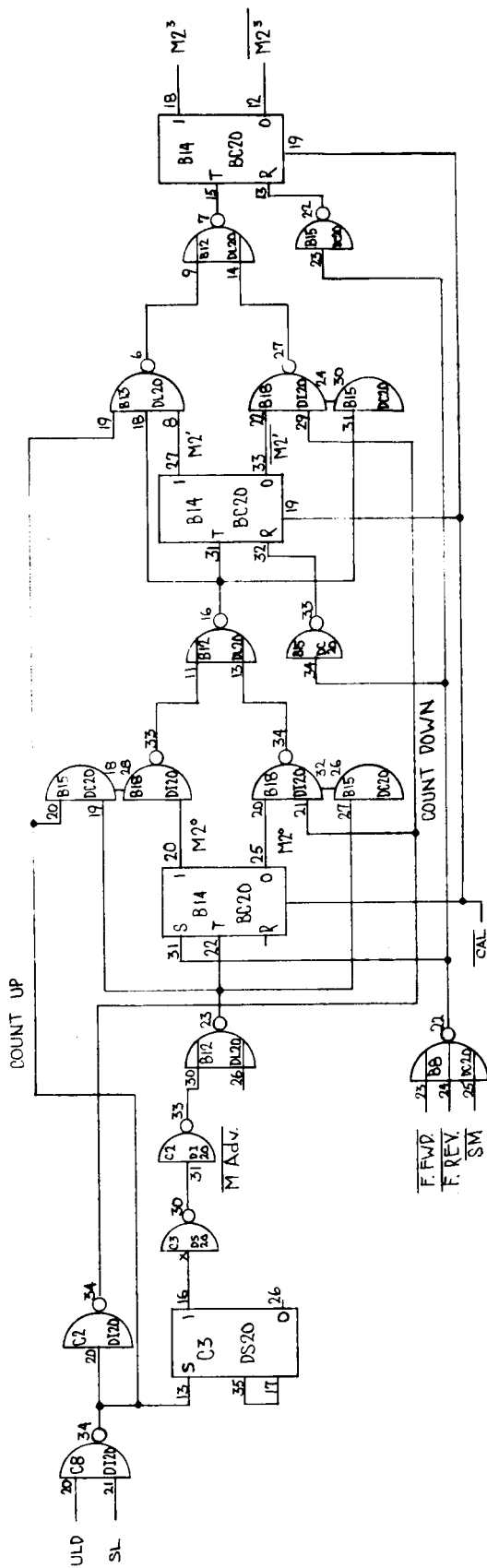




NOTE: RELAYS ARE MOUNTED BEHIND POWER
PANEL AT TOP OF RACK
SWITCHES ARE LOCATED IN FILM READER.

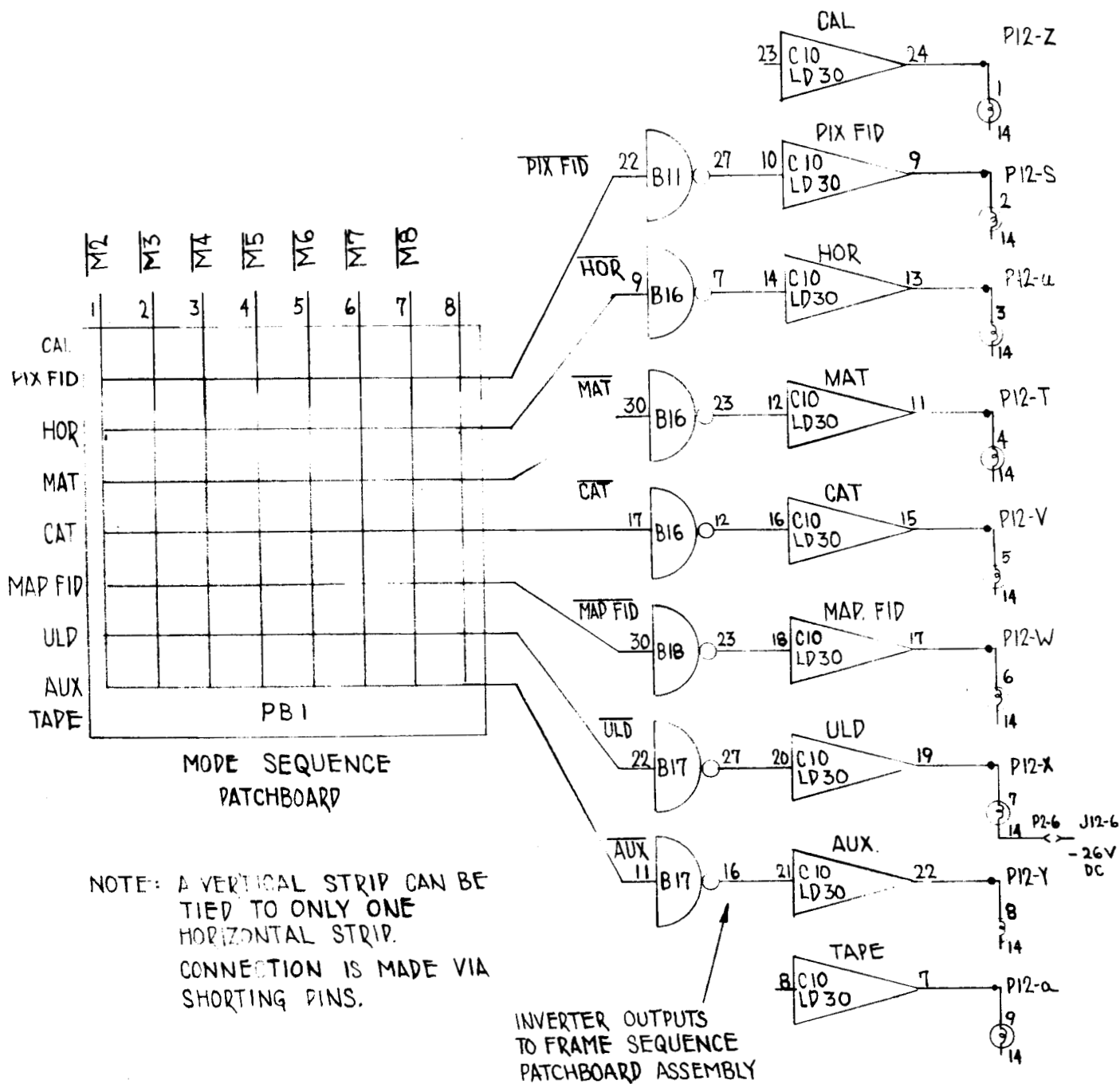
DRAWING NO.
9GB-05E

SWITCH-SIGNAL CONDITIONERS



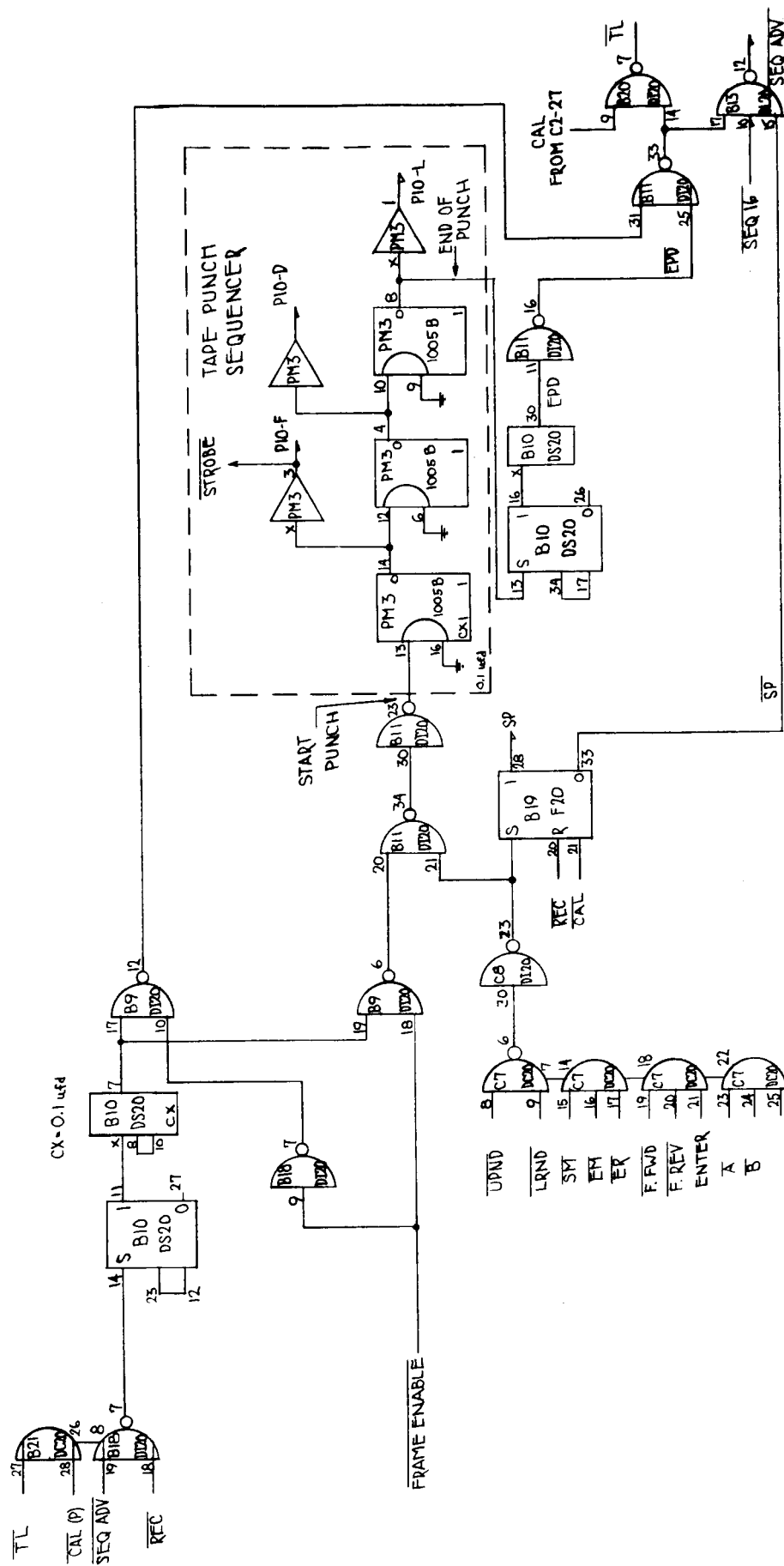
MODE COUNTER AND DIODE GATE DECODER

DRAWING NO.
998-06E



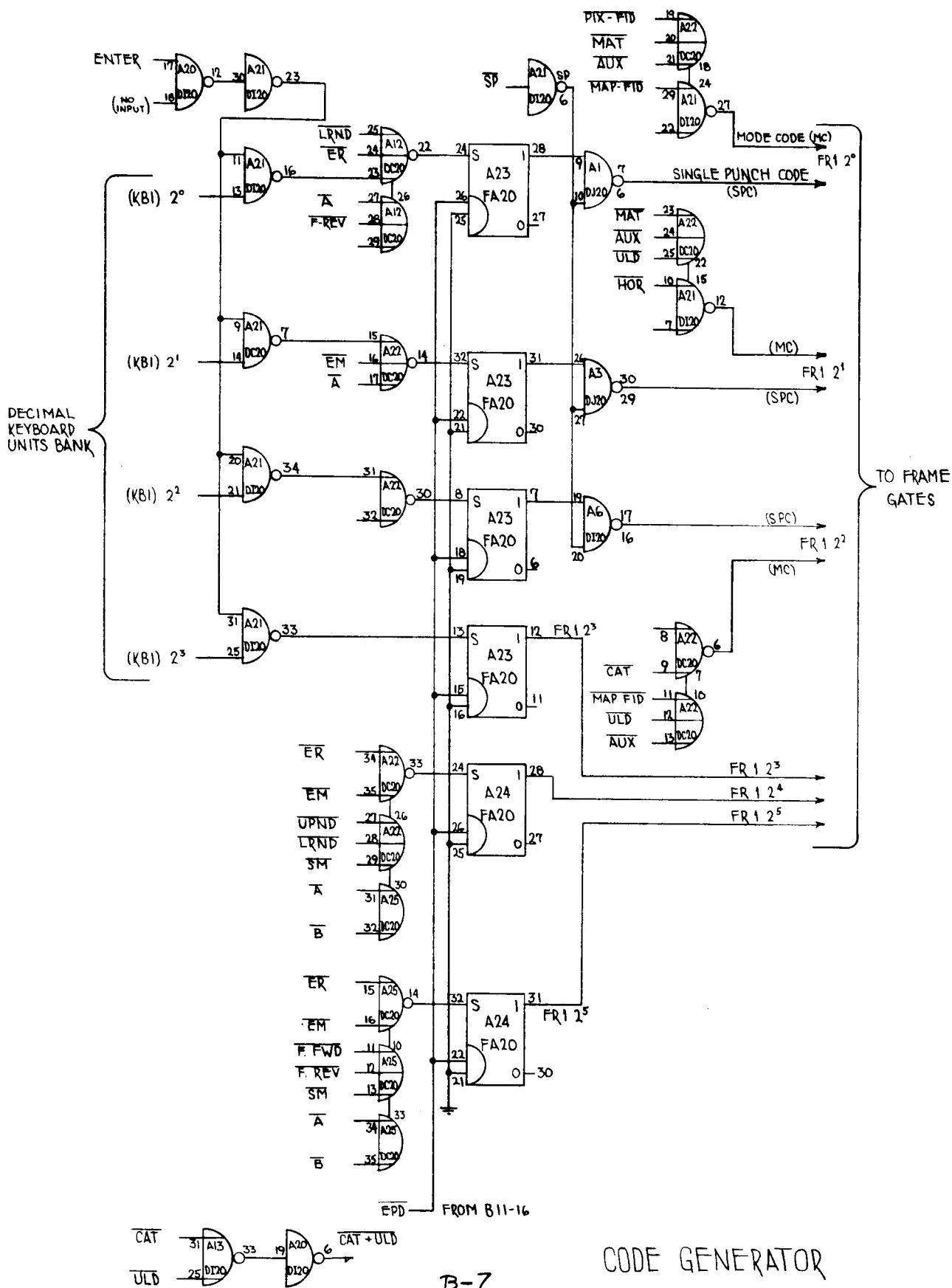
MODE SEQUENCE PATCHBOARD,
INVERTERS AND LAMP DRIVERS

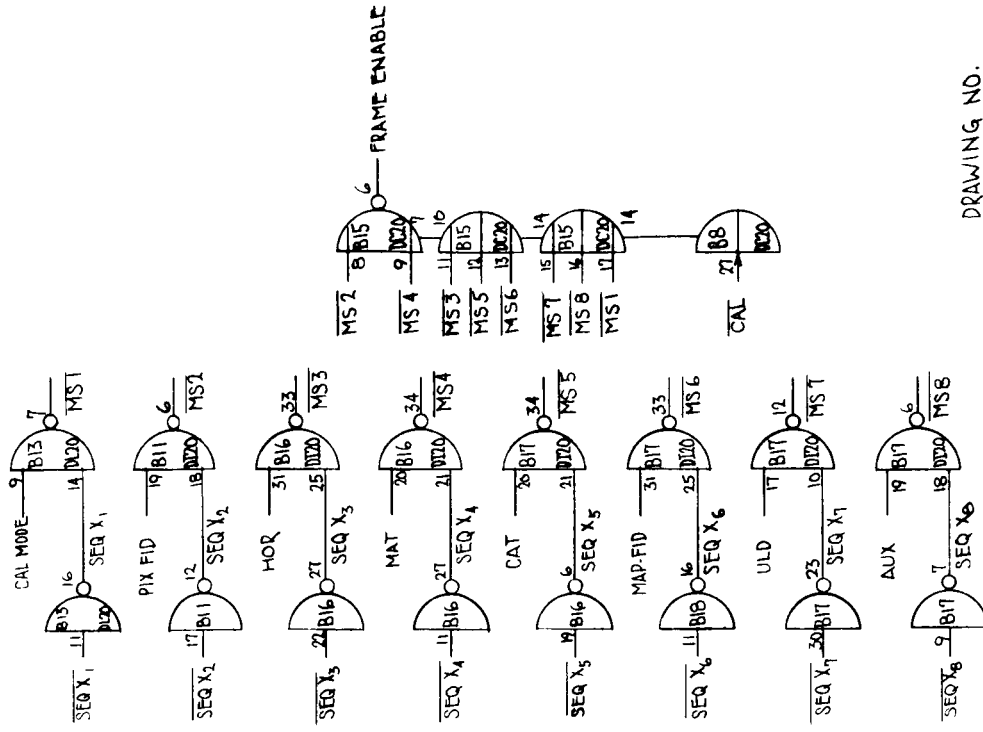
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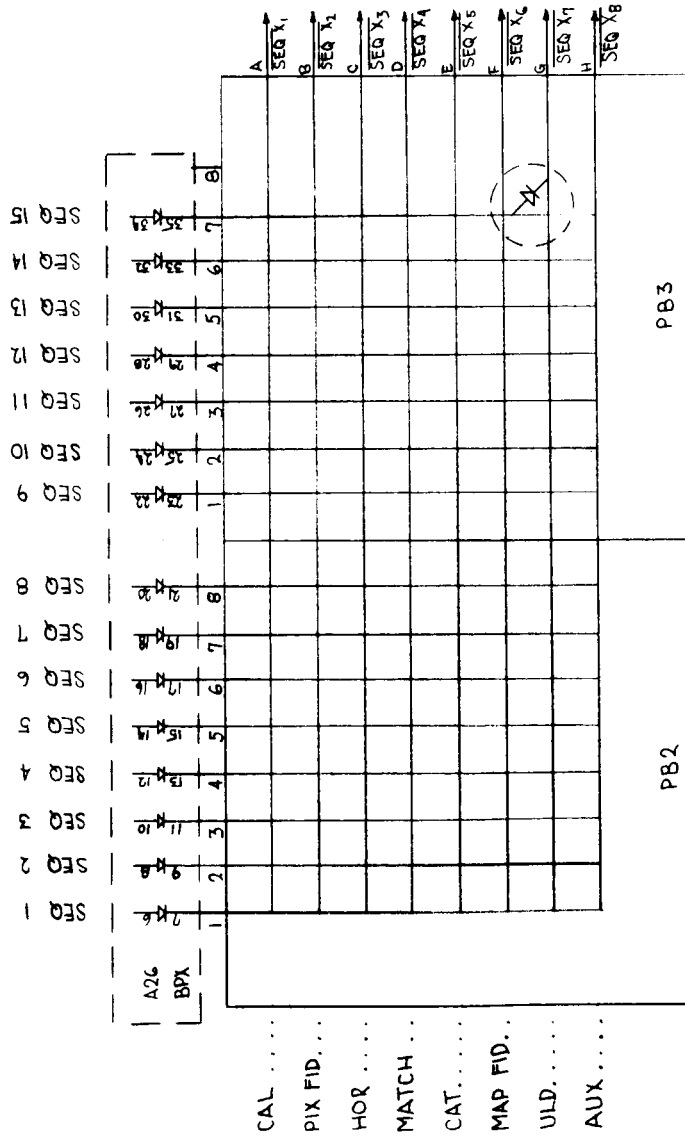
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968-08E

PUNCH CONTROL LOGIC

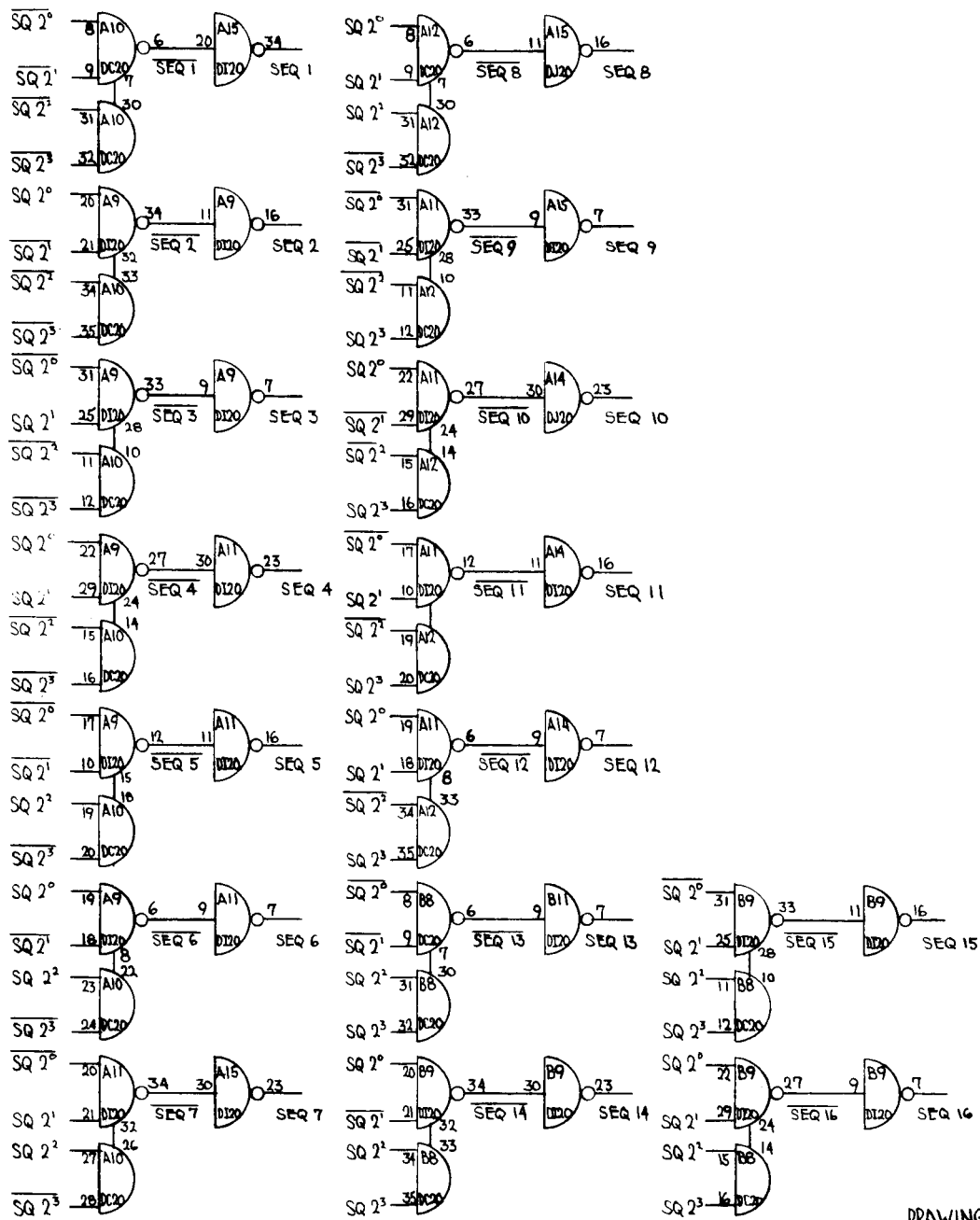
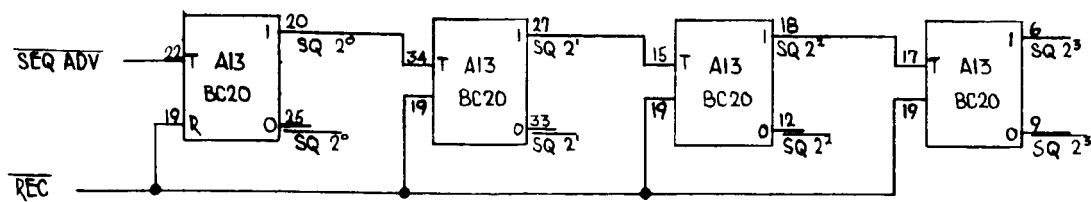




DRAWING NO.
9GB-10E

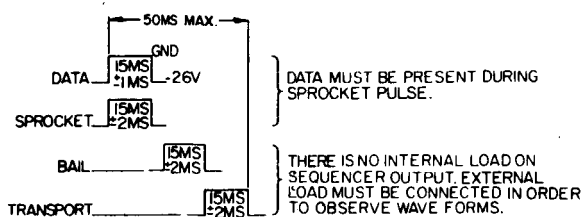
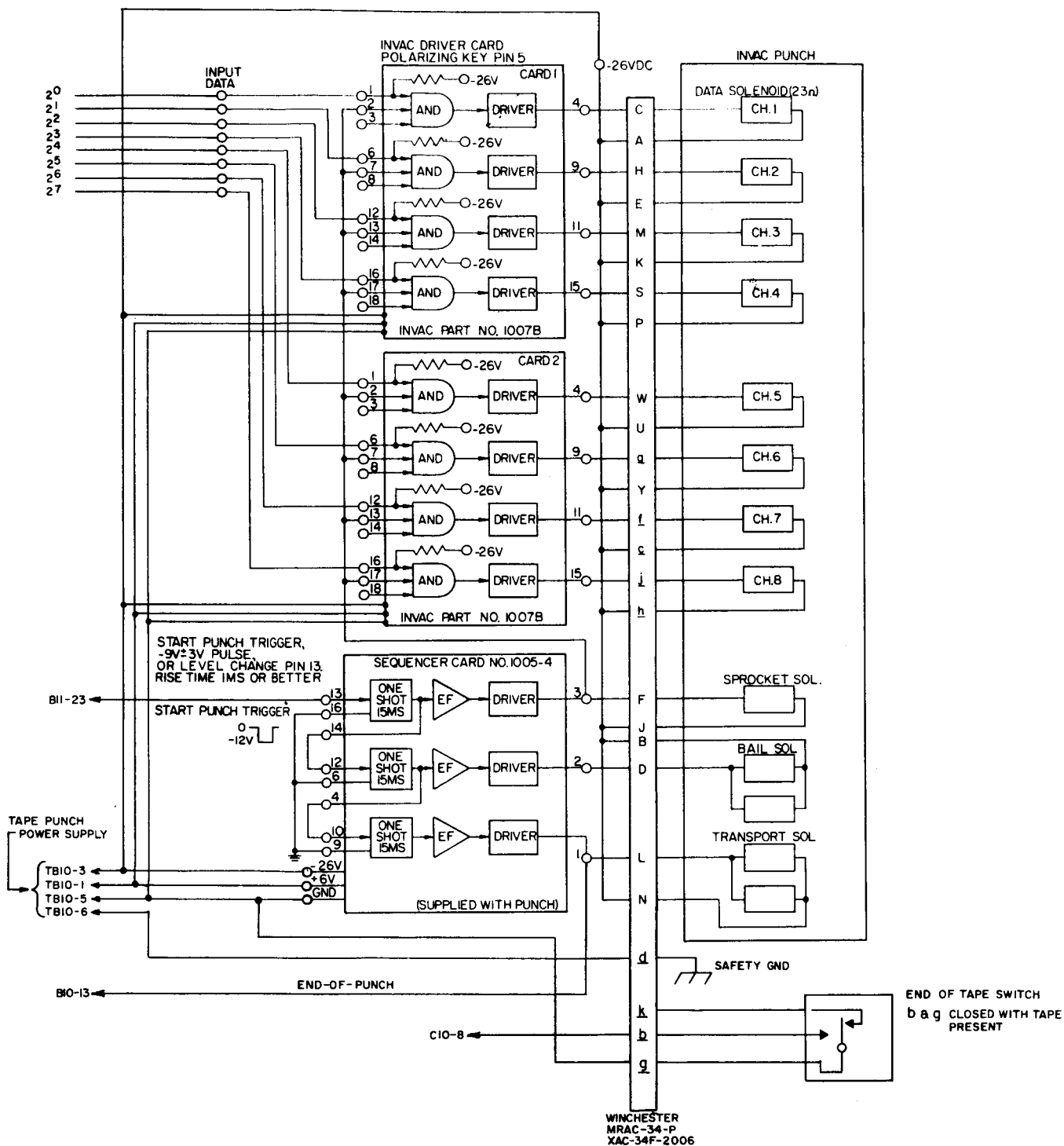


FRAME SEQUENCE PATCHBOARD ASSEMBLY



SEQUENCE COUNTER,
DIODE GATE DECODER, AND INVERTERS
B-9

DRAWING NO.
9GB-11E

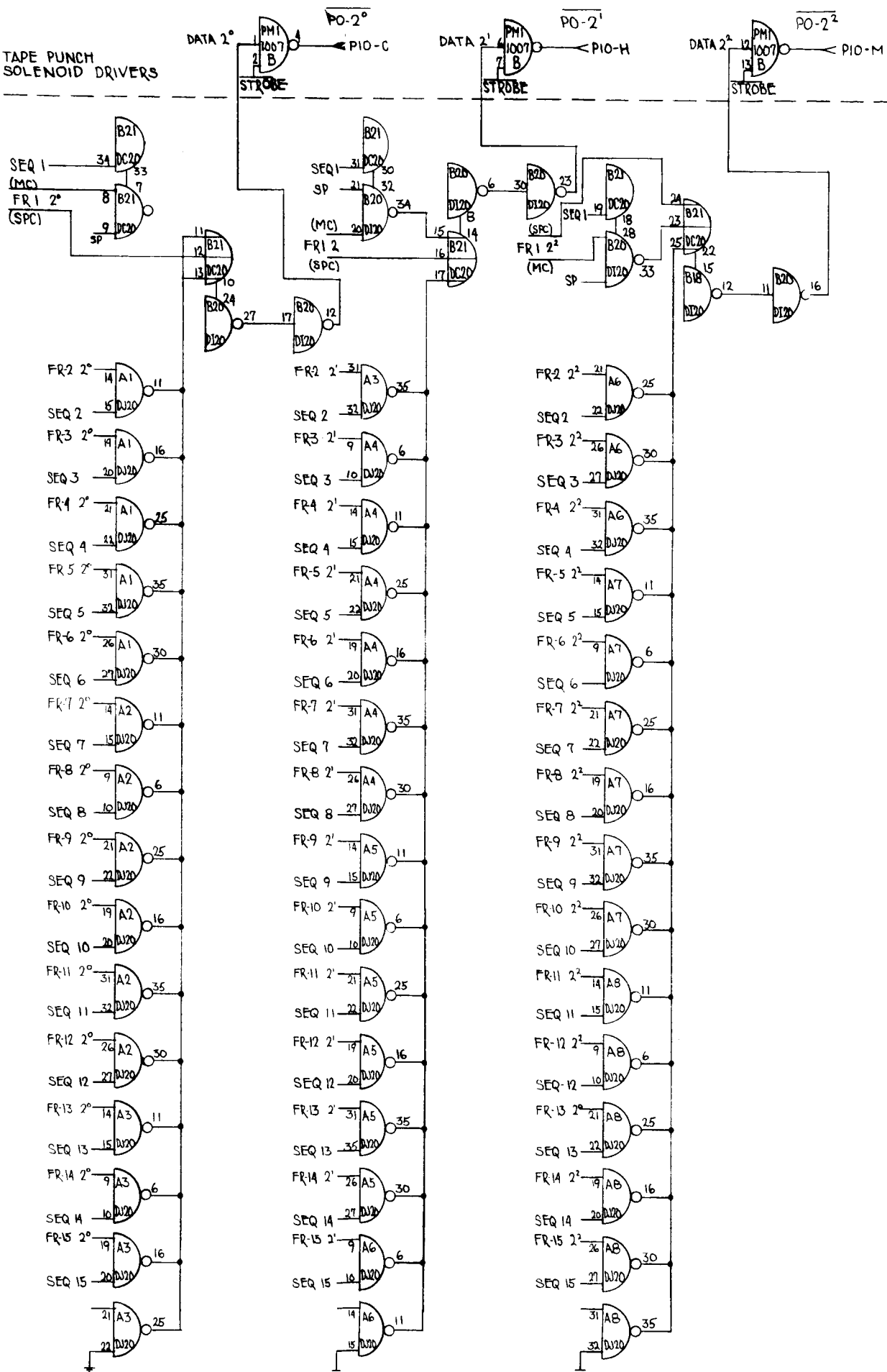


NOTES DRIVER CARD

1. DRIVER CARD OUTPUT 1.3AMP TO -26V±2V.
2. WHEN ALL INPUTS ARE LOGICAL ONE DRIVER OUTPUT GOES TO -0.8±0.4V WHEN LOADED.
3. LOGIC LEVELS
ONE -0.2V±0.2V
ZERO -9V±3V

DRAWING NO. 968-12E

TAPE PUNCH
SOLENOID DRIVERS

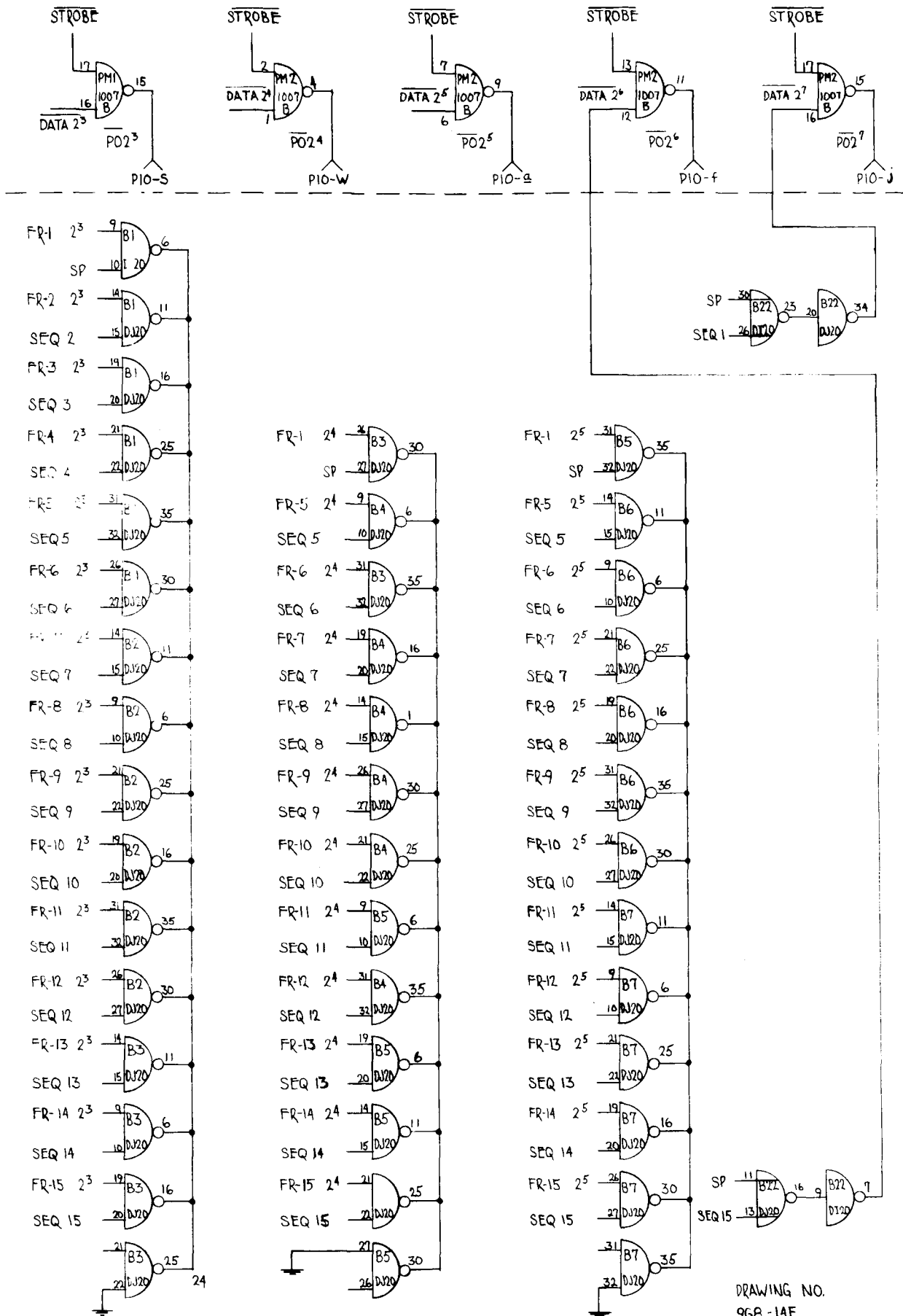


FRAME GATES, PUNCH LEVELS 1-3

B-11

DRAWING NO.
9G8-13E

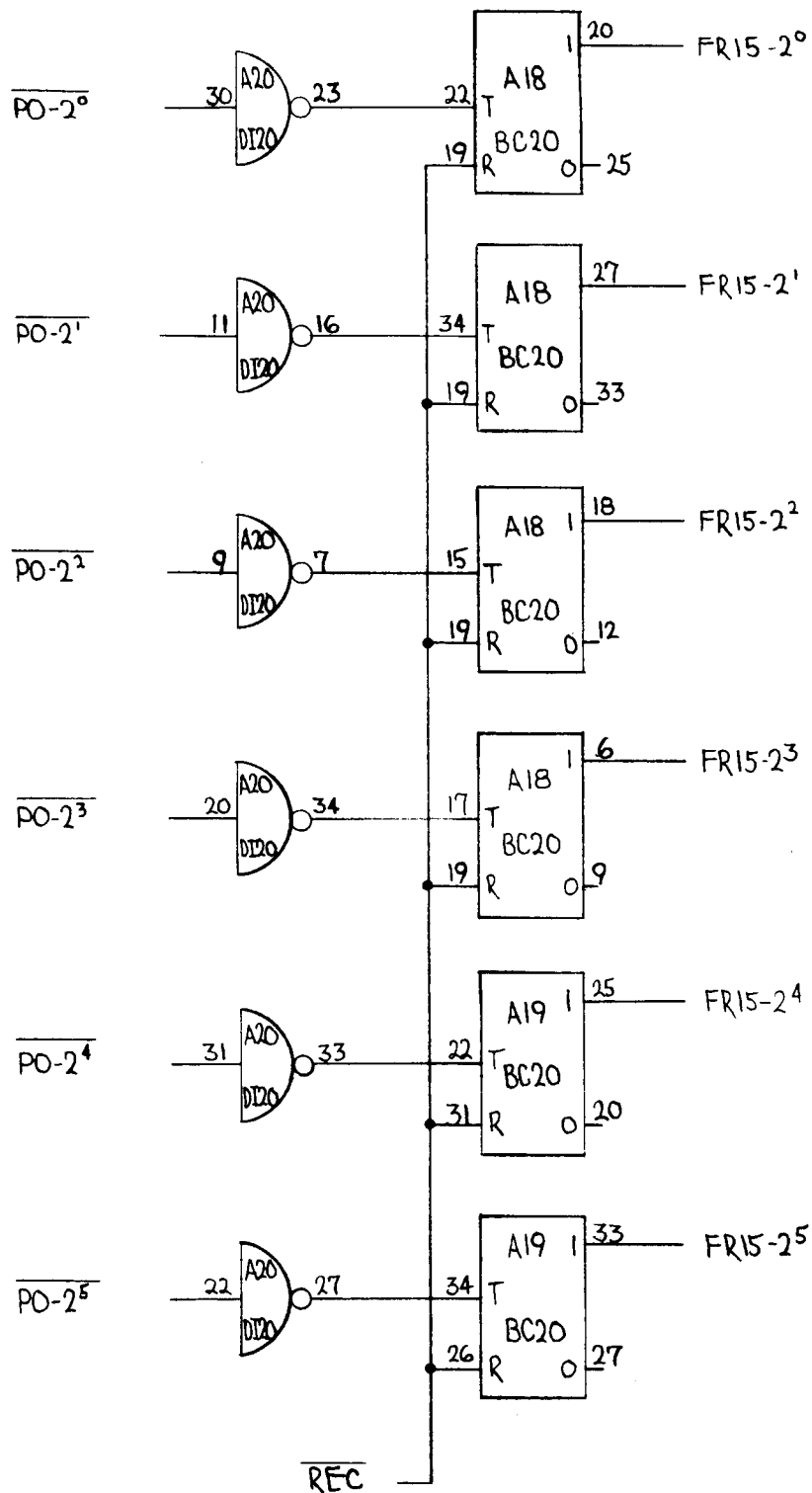
TAPE PUNCH SOLENOID DRIVERS



DRAWING NO.
9GB-14E

FRAME GATES, PUNCH LEVELS 4-8
B-12

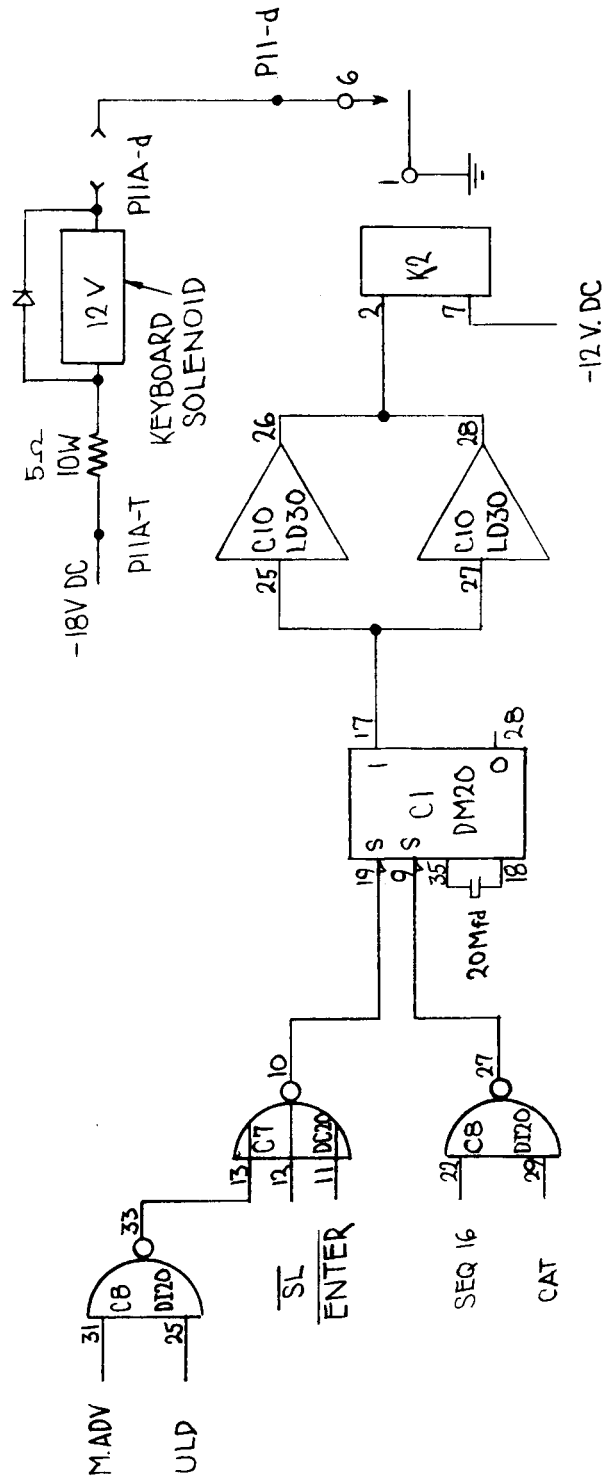
OUTPUTS
FROM
TAPE PUNCH
SOLENOID
DRIVERS



PARITY GENERATOR

B-13

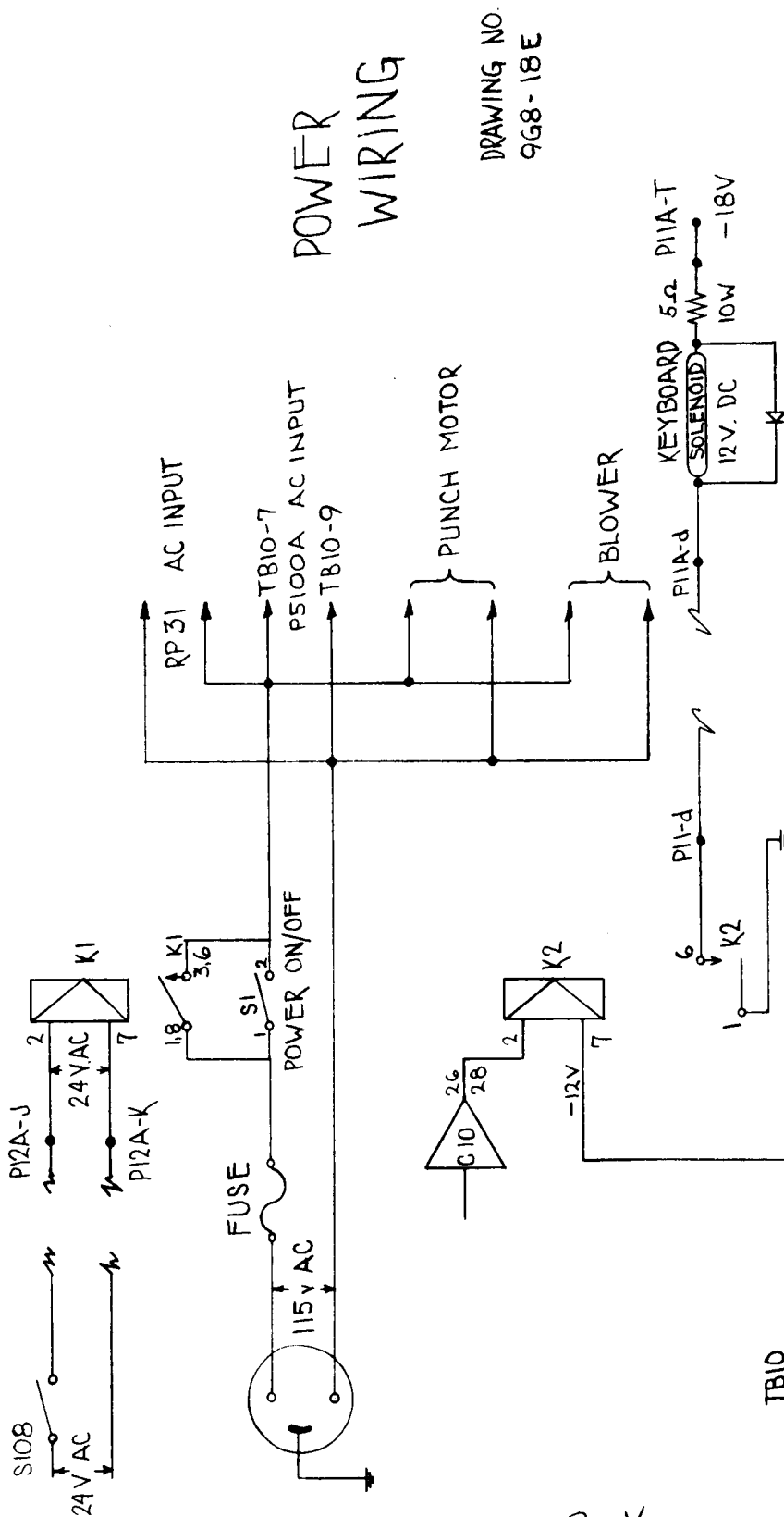
DRAWING NO.
9GB-15E



DRAWING NO.
968-16E

DECIMAL KEYBOARD RESET LOGIC

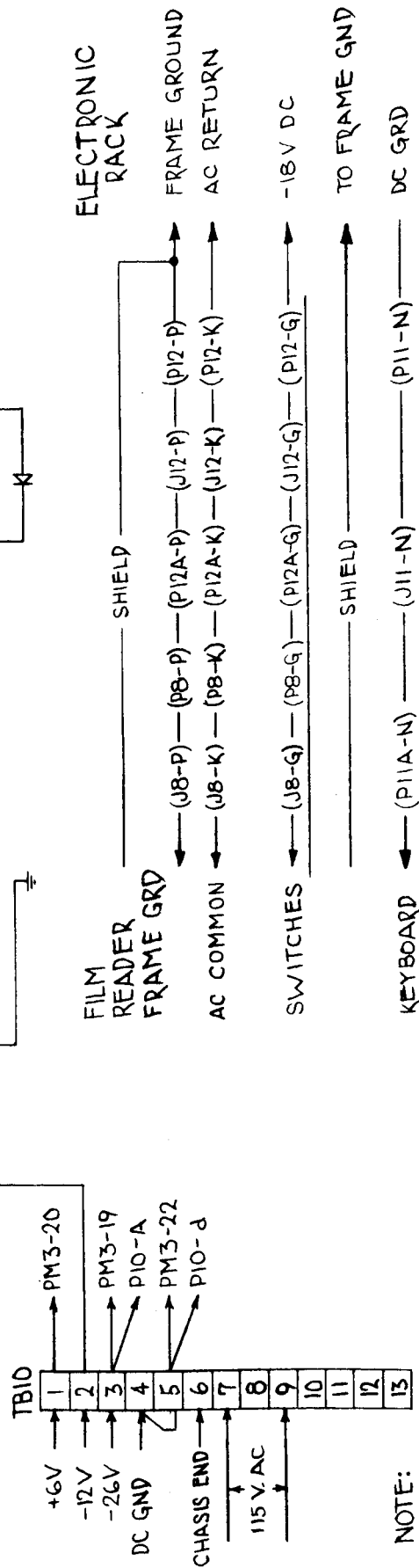
B-14



POWER WIRING

DRAWING NO.
968-18E

B-16



NOTE:

TB10 IS LOCATED AT REAR OF
TAPE PUNCH POWER SUPPLY

LOCATION OF DIGITAL MODULES

	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A			B	D	F	F	D	D	D	B	B			D	D	B	D	D	D	D	D	D	D	D	D	D	D	D
			P	C	A	A	C	I	I	C	C			I	I	C	C	I	C	I	J	J	J	J	J	J	J	J
			x	2	2	2	2	2	2	2	2			2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
				0	0	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
B			F	F	F		D	D	D	F	D	D	D	D	B	D	D	D	D	D	D	D	D	D	D	D	D	D
			F	F	F		C	C	I	F	I	I	I	C	C	L	L	I	S	I	C	J	J	J	J	J	J	J
			2	2	2		2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
			0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
C																			L		D	D				D	D	D
																			D	I	I	C	C			S	I	M
																			3	2	2	2	2			2	2	2
																			0	0	0	0	0			0	0	0

	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
D																												

* ENCODER REGISTER

NOTE: ABOVE VIEW IS FROM REAR
OF ELECTRONICS RACK

DRAWING NO.
9GB-19E

WIRE LIST - CABLE #11

<u>Rack</u>	<u>P11</u>	<u>J11</u>	<u>P11A</u>	<u>Film Reader Keyboard</u>
A21-13	A	A	A	(KB1) 2 ⁰ *
A21-14	B	B	B	2 ¹
A21-21	C	C	C	2 ²
A21-25	D	D	D	2 ³
A1-19	E	E	E	(KB2) 2 ⁰
A4-9	F	F	F	2 ¹
A6-26	G	G	G	2 ²
B1-19	H	H	H	2 ³
A1-21	J	J	J	(KB3) 2 ⁰
A4-14	K	K	K	2 ¹
A6-31	L	L	L	2 ²
B1-21	M	M	M	2 ³
DC GND	N	N	N	DC GND
B28-22	P	P	P	S203-NO
+12V.	R	R	R	+12V.
-6V.	S	S	S	-6V.
-18V.	T	T	T	-18V. †
C2-22	U	U	U	S201-NC
B27-20	V	V	V	S202-NC
B27-29	W	W	W	S203-NC
B27-9	X	X	X	S204-NC
B27-19	Y	Y	Y	S205-NC
B26-20	Z	Z	Z	S206-NC
B26-29	a	a	a	S207-NC
B26-9	b	b	b	S208-NC
B28-34	c	c	c	S202-NO
K2-6	d	d	d	-18V. return
B28-32	e	e	e	S204-NO
B28-30	f	f	f	S205-NO
B28-28	g	g	g	S206-NO
B28-26	h	h	h	S207-NO
B28-24	j	j	j	S208-NO

S202C, S203C, S204C, S205C, S206C, S207C, S208C, connected to DC GND.

S201-NC→-6V. S201-NO→GND.

* KB1, KB2, and KB3 correspond to sequencer input frames 2,3 and 4 respectively.

† Applied to solenoid for keyboard reset.

CABLE WIRE LIST - CABLE #12

<u>Rack</u>	<u>P12</u>	<u>J12</u>	<u>P12A</u>	<u>P8</u>	<u>J8</u>	<u>Film Reader</u>
B28-20	A	A	A	A	A	S101-NO
B28-18	B	B	B	B	B	S102-NO
B28-16	C	C	C	C	C	S103-NO
B28-14	D	D	D	D	D	S104-NO
B28-35	E	E	E	E	E	S105-NO
B28-10	F	F	F	F	F	S106-NO
-18V.	G	G	G	G	G	S101-C
C28-34	H	H	H	H	H	Spare
K1-2 [†] - 24 V. AC	J	J	J	J	J	S108-2 (24 V. AC)
K1-7 [†]	K	K	K	K	K	24 V. AC Com.
C28-32	L	L	L	L	L	Spare
C28-30	M	M	M	M	M	Spare
C28-28	N	N	N	N	N	Spare
Frame GND	P	P	P	P	P	Frame GND
C28-26	R	R	R	R	R	Spare
C10-9	S	S	S			IEE-2
C10-11	T	T	T			IEE-4
C10-13	U	U	U			IEE-3
C10-15	V	V	V			IEE-5
C10-17	W	W	W			IEE-6
C10-19	X	X	X			IEE-7
C10-22	Y	Y	Y			IEE-8
C10-24	Z	Z	Z			IEE-1
C10-7	a	a	a			IEE-9
-24V. DC	b	b	b			IEE-14
C28-8	c	c	c			Spare
C28-24	d	d	d			Spare
C28-22	e	e	e			Spare
C28-20	f	f	f			Spare
C28-18	g	g	g			Spare
C28-16	h	h	h			Spare
C28-14	j	j	j			Spare

* [S101C, S102C, S103C, S104C, S105C, S106C, S107C, connected together]

* (S106NO, S107NO connected together)

† K1 coil

APPENDIX C

DESCRIPTION OF DIGITAL MODULES

The following pages are excerpts from "Instruction Manual for 200-KC S-Pac Digital Modules" Computer Control Company, Inc., 5 August 1963.* All of the modules used in the Automated Attitude System are described in these pages. The figure and section division numbers used in this Appendix are those of the Computer Control Instruction Manual.

The special diode board BPX is shown at the rear of this section.

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200-KC S-PAC DIGITAL MODULES

SECTION II S-PAC MODULE SPECIFICATIONS

2-1 PRODUCT LINE SPECIFICATIONS

All listed S-PAC performance specifications are guaranteed minimums based on worst-case tolerances. Actual performance will invariably exceed these guaranteed minimums. In general, the 200-KC product line specifications are:

Frequency Range: DC to 200 KC (for all logic PACs)

Circuit speed is primarily determined by the time constant of the input circuit. This is chosen for optimum performance at 200 KC.

Noise Rejection: 1.5 V min (2 V typ) at ground level
1.4 min at -6 V level

NOTE

To obtain optimum noise rejection on DI, FF, FA, BC, and SR type PACs, jumper a 4-1/2-inch lead from pin 5 to pin 35. The jumper attenuates noise picked up by distributed impedance of the etched circuit.

Temperature Range: -20 to +55°C (+71°C local ambient)

Output Loading (Fan-Out):

All gates can drive 7 unit loads.

All flip-flops can drive 6 unit loads from each output.

All PAC outputs can drive 500 pf stray capacitance in addition to their rated loads.

Fan-In:

All input gates are expandable to 10 inputs.

2-2 SIGNALS

Logic Levels:

ONE (True): -5 to -6.5 V

ZERO (False): 0 to -1.5 V

200-KC S-PAC DIGITAL MODULES

Pulse Specifications:

To activate DC inputs: 1.5 μ sec min duration of applied ZERO

To activate AC inputs: 1.0 μ sec max rise time (10% to 90% or 6 V)
(Figure 2-2.1)

2.5 μ sec min width of the negative signal.
(Measured from 10% point on the falling edge to the 10% point on the rising edge.)

5.5 V min amplitude of the positive edge.

2-3 COMPONENTS

A minimum number of component types and values are incorporated in the circuit designs. In addition, all components are carefully chosen for reliable long life performance. Computer Control Company incoming inspection and quality control procedures ensure continuous quality standards.

2-4 DESIGN MARGINS

All circuit designs are based on worst-case assumptions in which the required transistor gain does not exceed 70 percent of end-of-life specified value. Diode and transistor voltage drops are considered for 0.1 volt greater than specified. Circuit design incorporates leakage factors at least twice the 71°C maximum leakage. Transistor and diode dissipation is less than 50 percent of the manufacturer's rated dissipation at 55°C.

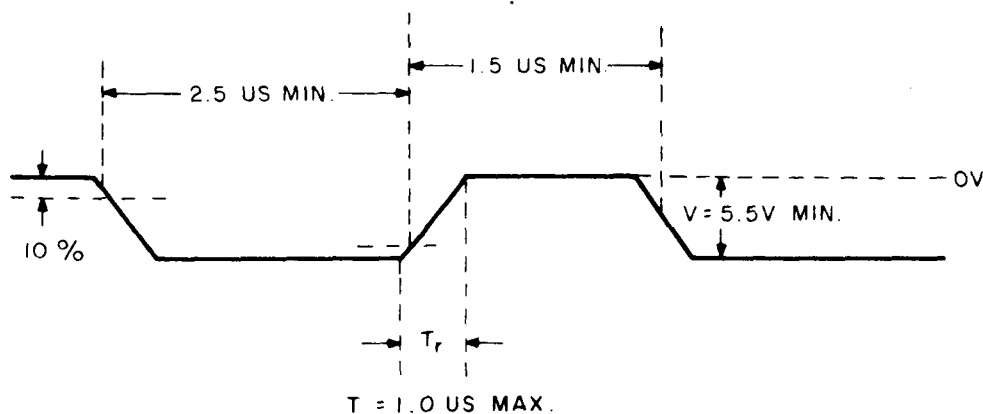


Figure 2-2.1. Trailing Edge Trigger Mode Signal Requirements

2-10

PEDESTAL GATE

Many PACs in the S-PAC line incorporate the pedestal gate. The basic gate has an AC input and a level control as shown in Figure 2-10.1.

The gate functions to turn off transistors on the positive transition of AC input signals if the voltage at the level control input is 0 volt.

Turnoff is accomplished by allowing a 6-volt charge to build up across the capacitor prior to the positive transition.

When the level control is 0 volt, point C is clamped at zero volt. When point A drops to -6 volts from ground, diode CR1 opens. Point B charges exponentially toward -18 volts with a time constant $R_1 C$. When the voltage at point B reaches -6 volts, diode CR1 conducts and clamps point B to -6 volts, the potential of point A.

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200-KC S-PAC DIGITAL MODULES

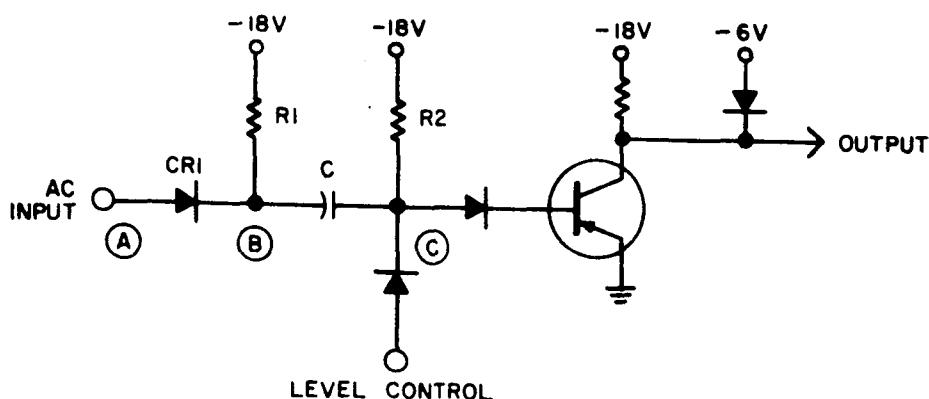


Figure 2-10.1. Single Pedestal Gate

When point A returns to 0 volt with a fast rise time, point C rapidly becomes +6 volts turning off the transistor. Point C then charges exponentially toward -18 volts with a time constant R_2C and becomes clamped to the level control voltage.

If the level control is held at -6 volts, the function of turning off the transistor is inhibited. In this case, point C is clamped to -6 volts. On the positive 6-volt transition at point A, point C rapidly becomes 0 volt which is not enough to turn off the transistor.

In summary, the circuit follows the two rules listed below:

1. To turn off the transistor: point B must be a -6 volts and point C must be at 0 volt prior to the positive transition of the AC input, point A.
2. To inhibit turning off the transistor: point C must be at -6 volts prior to the positive transition of the AC input, point A. Also, the amplitude of the positive transition should not exceed 6 volts.

For rule 1: To ensure that point B is -6 volts prior to the positive transition at point A, point A must be -6 volts for a designated time. This time is dictated by the time constant R_1C and the action of the potential at point B heading for -18 volts but clamping at -6 volts.

For rule 2: To ensure that point C is -6 volts prior to the positive transition, the level control voltage must be -6 volts prior to the negative transition of the AC input. In this case, when the AC input goes negative it pulls point C down with it.

200-KC S-PAC DIGITAL MODULES

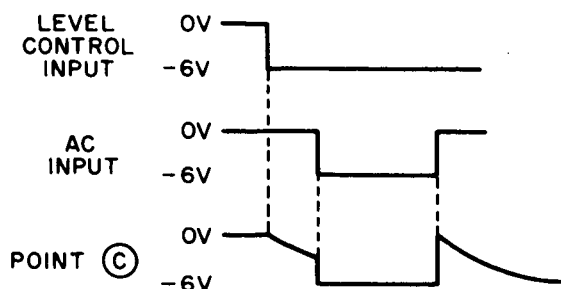


Figure 2-10.2. Waveforms for Transistor Turnoff

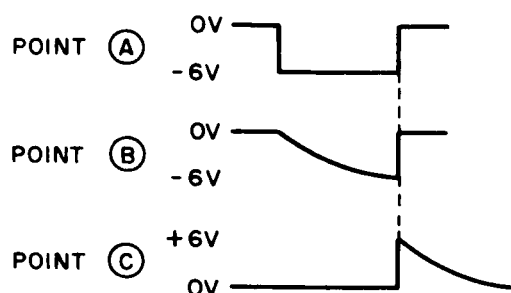


Figure 2-10.3. Waveforms to Inhibit Transistor Turnoff

Single pedestal gates are found on the UF-20 and FA-20 PACs as AC set and AC reset inputs. Also, circuit D of the BC-20 has a pedestal gate for its AC reset input. The AC set input of the FA-20, having its level control input not available, is a single pedestal gate. The level control for the gate is internally wired to the set output.

Common AC inputs, such as those on the BC-20 and SR-20, are essentially doubled pedestal gates as shown in Figure 2-10.4. In the BC-20 and SR-20, the set and reset outputs are wired back as the level controls.

In this circuit the set and reset level controls perform the function of steering the AC input signal to the proper side of the flip-flop. Normally, one level control input is at zero volt and the other is -6 volts. The level control at zero volt must conform to rule 1; the level control at -6 volts must conform to rule 2.

Double pedestal gates differ from single pedestal gates because, to fulfill rule 1, the AC input must be negative twice as long to allow point B to charge to -6 volts (this is necessary because the time constant $R_1 \times 2C$ is twice as large).

200-KC S-PAC DIGITAL MODULES

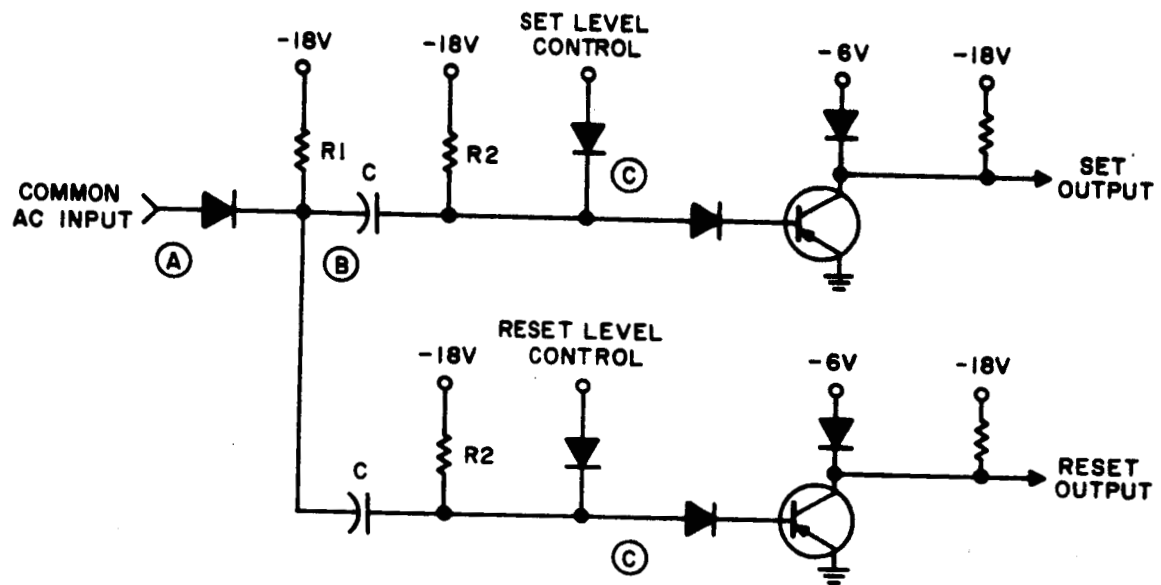


Figure 2-10.4. Double Pedestal Gate

3-1

COUNTER PAC, MODEL BC-20

GENERAL DESCRIPTION. Counter PAC, model BC-20 contains four independent, 200-KC counter stages that can be wired for binary or binary-coded-decimal (BCD) operation. Internally provided gating allows 8421 BCD counting, as well as divide-by-six and other feedback counting modes (Figures 3-1.1 through 3-1.3). Parallel drop-in to the counter is possible in both modes. The BC-20 (Figures 3-1.4 and 3-1.5) can be used to implement UP-DOWN counters, instantaneous carry counters, etc., by use of external S-PAC logic. The individual BC-20 flip-flops can also be used as independent complementing flip-flops.

Each stage has a complement input that employs either leading- or trailing-edge triggering. Trailing-edge triggering allows the counter output to be gated with a count signal pulse without the need for delay circuits or 2-phase clocks.

CIRCUIT FUNCTION. The four basic flip-flop circuits (Figure 3-1.6) on each BC-20 PAC are functionally identical to that of the FF-20; the DC inputs have the same effect. One DC set input plus node is provided for each flip-flop. If reset logic is desired, diode clusters may be wired to the reset node.

a. Common Reset. A 10- μ sec positive pulse applied to the common reset input clears (resets) the four counter stages simultaneously.

b. Complement Input (see Paragraph 2-10). The complement input is an AC-coupled input sensitive to positive steps. For trailing-edge counting or complementing, negative signals of 2.5- μ sec minimum duration should be used. For leading-edge triggering, positive signals of 1.5- μ sec minimum duration are required, with the requirement that the positive signals represent at most a 50 percent duty factor at 200 KC. At any count rate and in any mode, a 2.5- μ sec minimum negative input pulse is required for proper counter operation.

In general, only one logic operation can be performed on a BC-20 in any 5- μ sec interval. An exception is the DC set and reset inputs, which can be operated twice in a 5- μ sec interval.

c. Gated Complement Input. The second stage of the BC-20 has a gated complement input for use in BCD and binary counters. When either is

200-KC S-PAC DIGITAL MODULES

at ONE (-6 V), or open, a positive transition at the other input produces the same effect as a simple complement input. Thus, either diode can be used as a simple complement input. When one input is already at ground level, a positive transition on the other input has no effect. In BCD mode, this gate inhibits the carry into the second stage on the 10th count.

d. Gated AC Reset. The fourth stage of the counter is provided with a gated AC reset input. A positive transition applied to either diode when the counter stage is in the set condition resets the stage. In BCD mode, this gate resets the fourth stage on the count of 10.

NOTE

In all applications of the BC-20, pin 35 should be connected to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS.

Input Loading

DC inputs: 1 unit load each

Common reset: 4 unit loads each

Complement inputs: 2 unit loads each

AC reset input: 2 unit loads each

Circuit Delay

1.2 μ sec (max propagation time)

0.6 μ sec (typ propagation time)

Output Drive Capability

6 unit loads plus 500 pf stray capacitance each

Total Power

1.3 W

Polarization

Pins 28 and 30

Timing

See Figures 3-1.1 through 3-1.3

Frequency of Operation

DC to 200 KC (max)

Output Waveform Characteristics

Rise time: 0.5 μ sec (typ)

Fall time: 0.8 μ sec (typ)

Current Requirements

-18 V: 56 ma

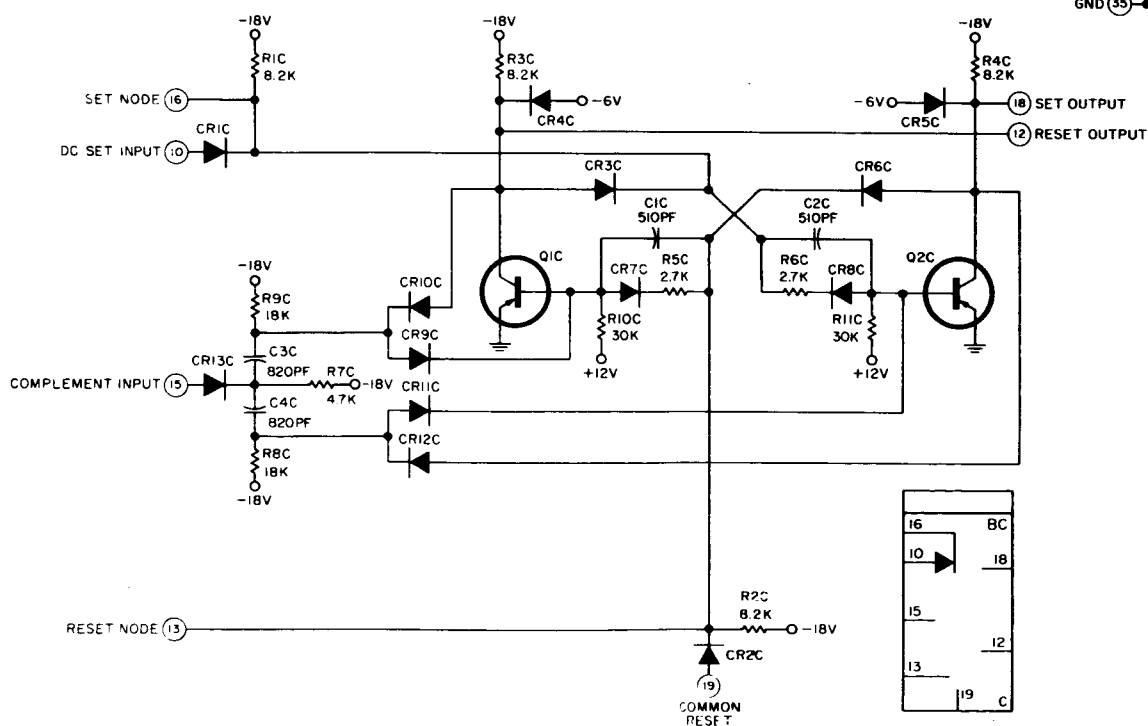
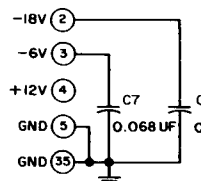
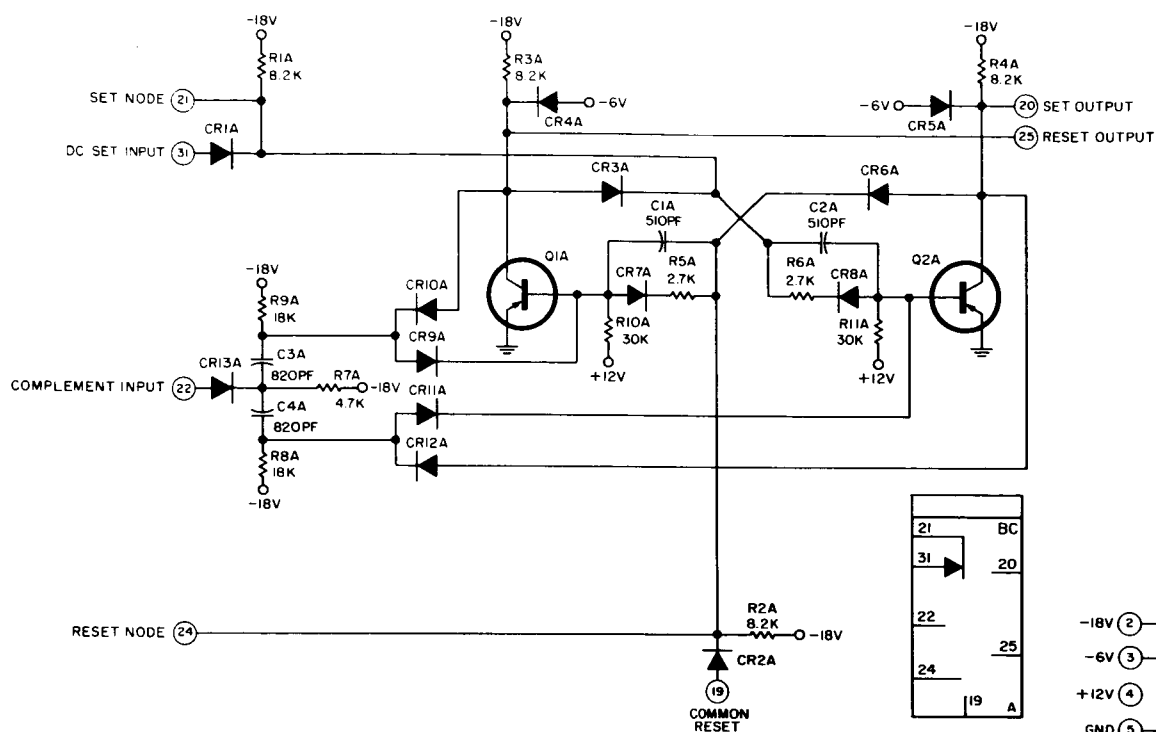
-6 V: 24 ma (reverse current into supply)

+12 V: 3.5 ma

Handle Color Code

Long: Blue

Short: Orange



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C-10

200-KC S-PAC DIGITAL MODULES



**Figure 3-1.6. Counter PAC, BC-20,
Schematic and Block Diagram**

200-KC S-PAC DIGITAL MODULES

3-6

DIODE PAC, MODEL DC-20

GENERAL DESCRIPTION. Diode PAC, model DC-20 (Figure 3-6.1), contains one 2-input NAND gate, five 3-diode clusters, and two 2-diode clusters. The DC-20 NAND gate input can be expanded by adding the diode clusters; the diode clusters can be used to expand the inputs to other S-PAC circuits.

CIRCUIT FUNCTION. The DC-20 NAND gate (Figure 3-6.2) consists of a 2-input gate, followed by the transistor inverter amplifier. When all inputs are at ONE (-6 V), the gate turns the transistor on and the output is clamped through the transistor to zero volt. When any input goes to zero volt, the transistor is turned off and the output falls to the clamp voltage of -6 volt.

The diode clusters can be wired to the node input of any S-PAC for expansion of its inputs up to a maximum of ten. Care should be taken to assure that diode cluster connections are made to local S-PACs and that the interconnecting leads are not cabled. Recommended maximum lead length is 1-1/2 feet.

SPECIFICATIONS.

Input Loading

1 unit load each

Circuit Delay (measured at
-3 V, averaged over two
stages)

0.6 μ sec (max)

0.3 μ sec (typ)

Output Drive Capability

7 unit loads and 500 pf stray
capacitance each

Polarization

Pins 14 and 16

Total Power

0.1 W

Frequency of Operation

DC to 200 KC (max)

Output Waveform Characteristics

Rise time: 0.5 μ sec (typ)

Fall Time: 0.8 μ sec (typ)

Current Requirements

-18 V: 4 ma

-6 V : 2 ma (reverse current into
supply)

+12 V: 0.5 ma

Handle Color Code

Long: Red

Short: Blue

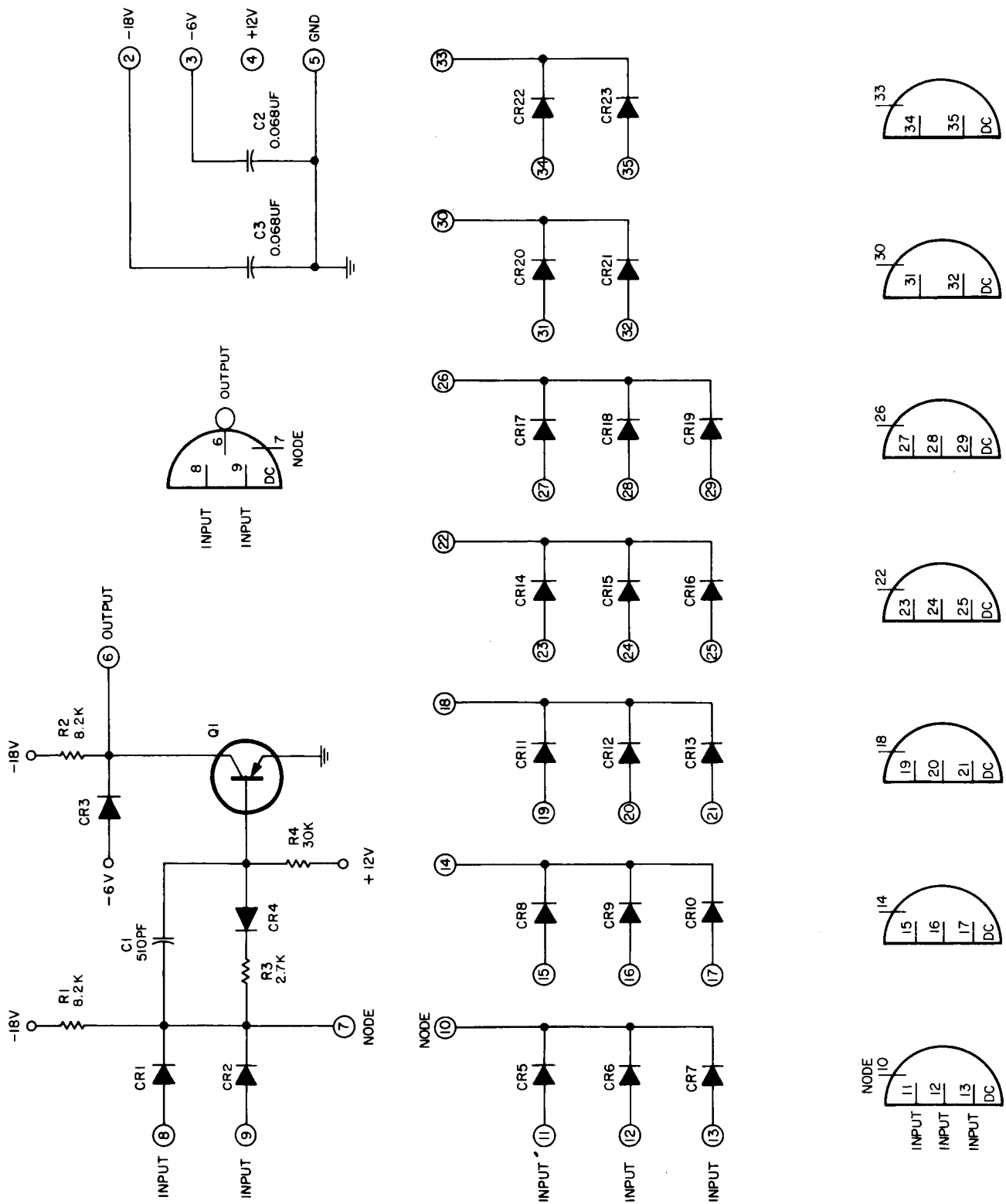


Figure 3-6.2. Diode PAC, DC-20, Schematic and Block Diagram

200-KC S-PAC DIGITAL MODULES

3-8

NAND PAC, MODEL DI-20

GENERAL DESCRIPTION. The NAND PAC, model DI-20, (see Figures 3-8.1 and 3-8.2) contains eight 2-input NAND gates. These gates are expandable up to a maximum of 10 inputs by connecting diode clusters contained in the DC or DN S-PACs. Five gates have a node input for expansion. The other three gates may be expanded by using one of their diode inputs as a node. (When so used, noise margins on expanded inputs are reduced by 0.3 volt.)

Each NAND gate performs the NAND function for negative voltage logic (ONE = -6 V), or the NOR function for positive voltage logic, (ONE = 0 volt). The gates operate on levels, pulses, or with combinations of both.

Two DI-20 NAND gates form a flip-flop when their inputs and outputs are cross-coupled.

CIRCUIT FUNCTION. Each DI-20 circuit (Figure 3-8.3) consists of a 2-input gate, followed by a transistor inverter amplifier. When all inputs are at ONE (-6 V), the gate turns the transistor on and the output is clamped through the transistor to zero volt. When any input goes to ZERO (0 V), the transistor is turned off and the output falls to the clamp voltage of -6 volts.

NOTE

For all applications of the DI-20, pin 35 should be jumpered to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

200-KC S-PAC DIGITAL MODULES

SPECIFICATIONS.

Input Loading

1 unit load each

Circuit Delay (measured at
-3 V averaged over two stages)

0.6 μ sec (max)

0.3 μ sec (typ)

Output Drive Capability

7 unit loads and 500 pf stray
capacitance each

Polarization

Pins 28 and 32

Total Power

0.6 W

Frequency of Operation

DC to 200 KC (max)

Output Waveform Characteristics

Rise time: 0.5 μ sec (typ)

Fall time: 0.8 μ sec (typ)

Current Requirements

-18 V: 30 ma

-6 V: 12 ma (reverse current
into supply)

+12 V: 3.5 ma

Handle Color Code

Long: Red

Short: Yellow

200-KC S-PAC DIGITAL MODULES

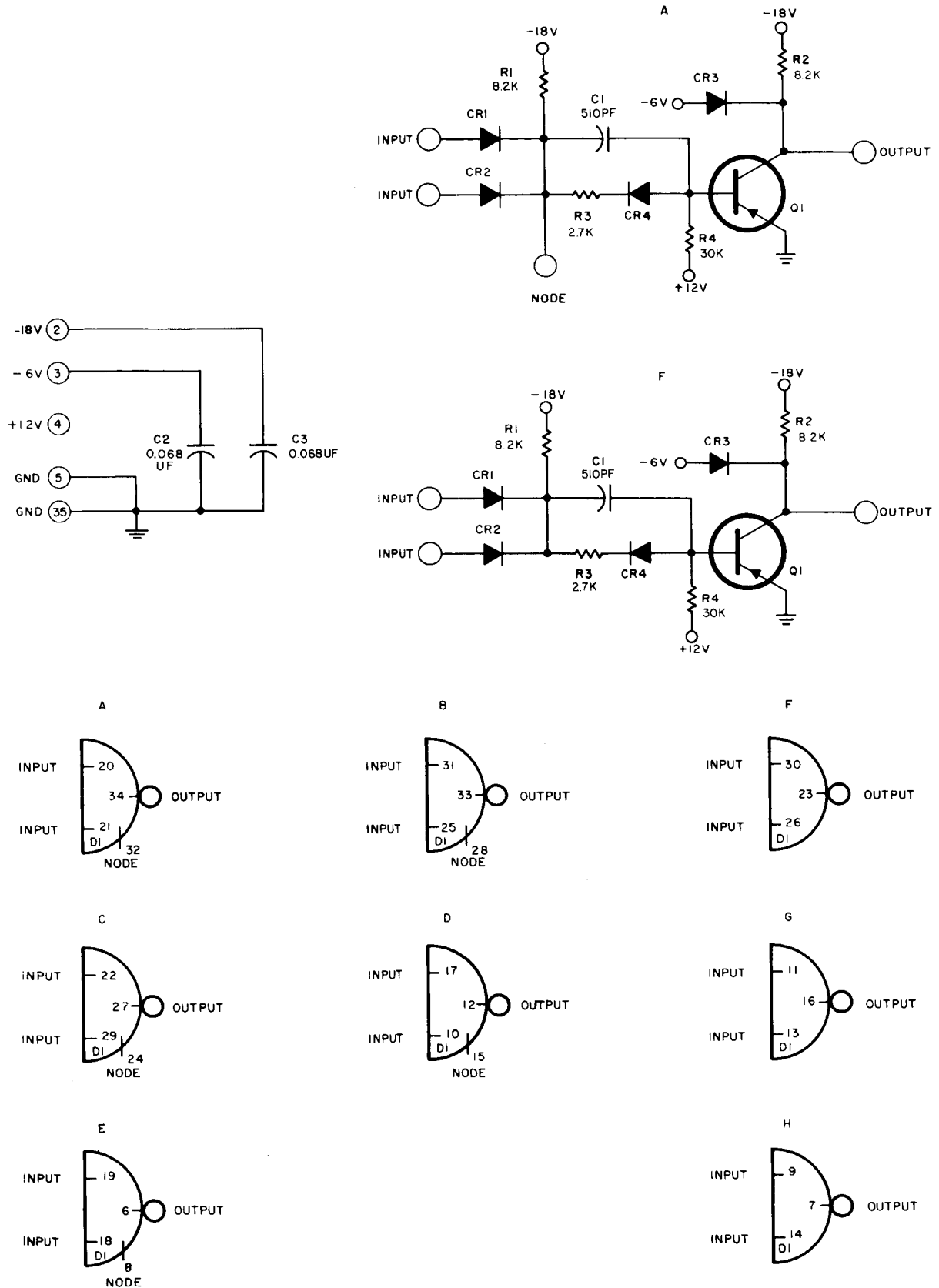


Figure 3-8.3. NAND PAC, DI-20, Schematic and Block Diagram

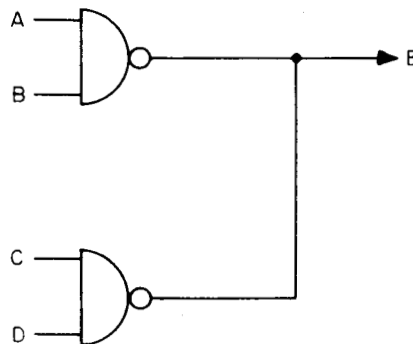
200-KC S-PAC DIGITAL MODULES

3-9

PARALLEL NAND PAC, MODEL DJ-20

GENERAL DESCRIPTION. Parallel NAND Gate PAC, model DJ-20 (Figure 3-9.1) contains six 2-input NAND gates with nodes, and separate collector resistors to provide gate paralleling capability. The PAC is designed to allow flexibility for optimum logic in applications such as decoding, parity generation, multiplexing, etc. The circuits are standard S-PAC NAND gates similar to those of the DF-20 PAC.

NAND gates with parallel collectors perform logic functions as follows.



$$E = \overline{AB \vee CD}$$

CIRCUIT FUNCTION. The DJ-20 (Figure 3-9.2) contains six 2-input NAND gates with separate load circuits. A load circuit consists of a pull-up resistor to the -18 volts supply and a clamp diode to -6 volts. Each collector load may be jumpered to a corresponding gate circuit to form a standard NAND gate; however, a single load circuit may be tied to the output of several parallel connected gate circuits without affecting the fanout. If the inputs are such that only one transistor is conducting, the output will be at zero volt. The maximum drive capability, regardless of how many collector outputs are jumpered in parallel, is 7 unit loads as shown in the following illustration.

200-KC S-PAC DIGITAL MODULES

SPECIFICATIONS.

Input Loading

1 unit load each input

Circuit Delay (measured at
-3 V, averaged
over two stages)

0.6 μ sec (max)

0.3 μ sec (typ)

Output Drive Capability

7 unit loads each output

Total Power

0.5 W (max)

Polarization

Pins 20 and 30

Frequency of Operation

DC to 200 KC (max)

Output Waveform Characteristics

Rise time: 0.5 μ sec (typ)

Fall time: 0.8 μ sec (typ)

Current Requirements

-18 V: 23 ma

-6 V: 9 ma (reverse current
into supply)

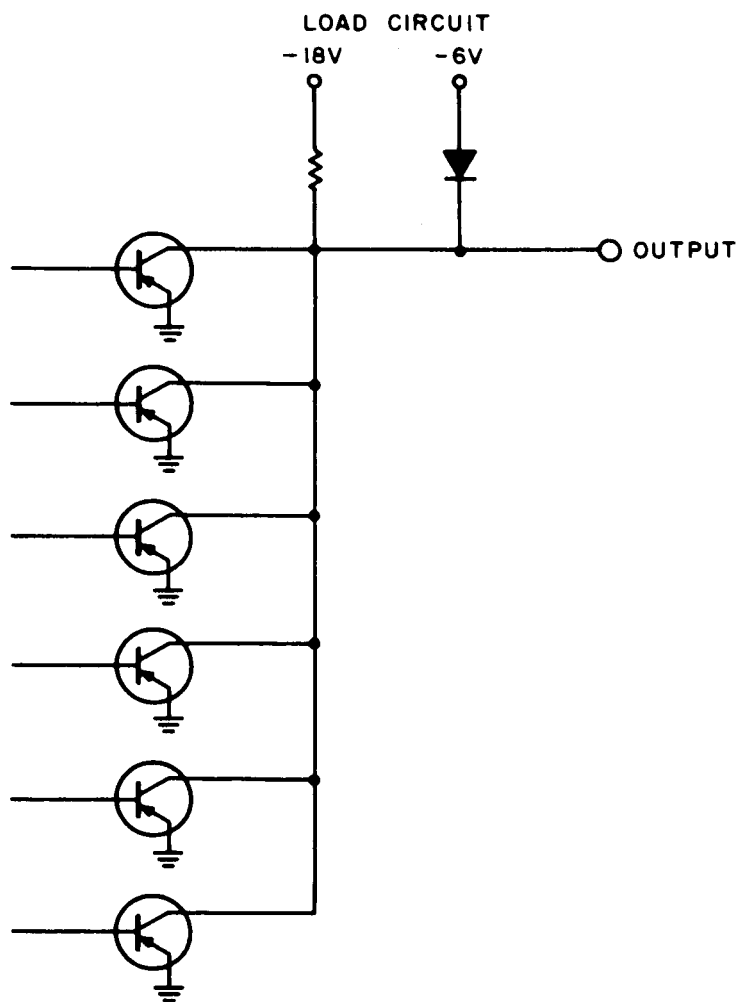
+12 V: 2.5 ma

Handle Color Code

Long: Red

Short: Brown

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Model DJ-20 Parallel Gate Configuration

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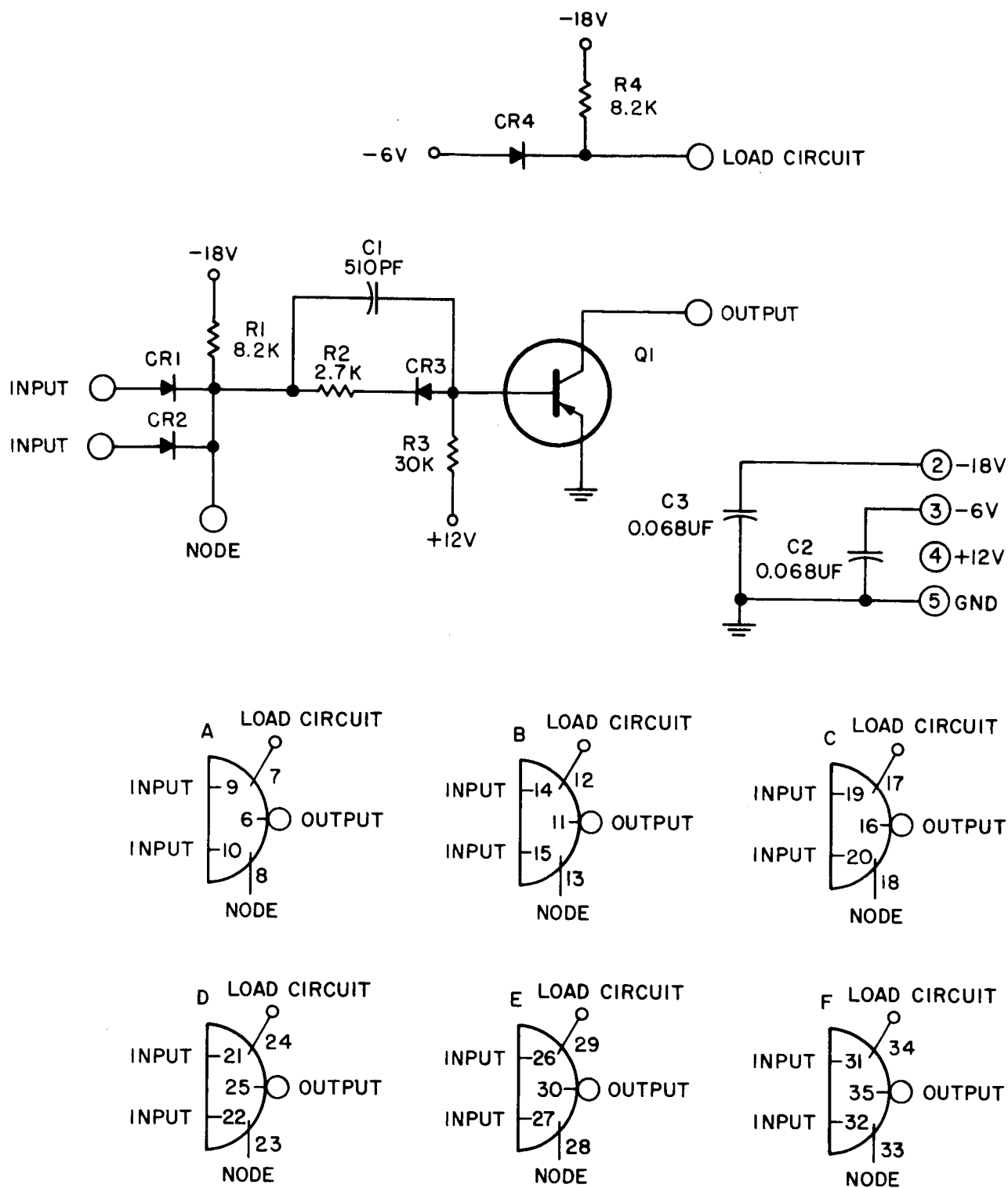


Figure 3-9.2. Parallel NAND PAC, DJ-20, Schematic and Block Diagram

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3-9A

NAND PAC, MODEL DL-20

GENERAL DESCRIPTION. NAND PAC, model DL-20, (Figures 3-9A.1 and 3-9A.2) contains five 3-input and three 2-input NAND gates with-out nodes. The gates may be expanded by using one for the diode inputs as a node and connecting diode clusters from a DC, DN, or DF S-PAC. However, the use of a diode input as a node slightly reduces noise margins on the ex-panded inputs (from the S-PAC noise margin minimum of 1.5 volts to 1.2 volts).

Each NAND gate performs the NAND function for negative voltage logic (ONE = -6 V), or the NOR function for positive voltage logic, (ONE = 0 volt). The gates operate on levels, pulses, or with combinations of both.

Two DL-20 NAND gates form a flip-flop when their inputs and out-puts are cross-coupled.

The DI-20 and DL-20 are similar PACs with identical input and output connector pins and are, therefore, interchangeable in S-BLOC installation.

The difference between the PACs is that the DI-20 contains five gates with a 2-diode and 1-node input and the DL-20 contains five gates with 3-diode inputs.

CIRCUIT FUNCTION. Each DL-20 circuit (Figure 3-9A.3) consists of five 3-input and three 2-input gates followed by a transistor inverter ampli-fier. When all inputs are at ONE (-6 V), the gate turns the transistor on and the output is clamped through the transistor to 0 volt. When any input goes to ZERO (0 V), the transistor is turned off and the output falls to the clamp volt-age of -6 volts.

NOTE

For all applications of the DL-20, pin 35 should be jumpered to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

200-KC S-PAC DIGITAL MODULES

SPECIFICATIONS.

Input Loading

1 unit load each

Circuit Delay (measured at -3 V averaged over two stages)

0.6 usec (max)

0.3 usec (typ)

Output Drive Capability

7 unit loads and 500 pf
capacitance each

Polarization

Pins 28 and 32

Total Power

0.6 W

Frequency of Operation

DC to 200 KC (max)

Output Waveform Characteristics

Rise time: 0.5 usec (typ)

Fall time: 0.8 usec (typ)

Current Requirements

-18 V: 30 ma

- 6 V: 12 ma (reverse current
into supply)

+12 V: 3.5 ma

Handle Color Code

Long: Orange

Short: Red

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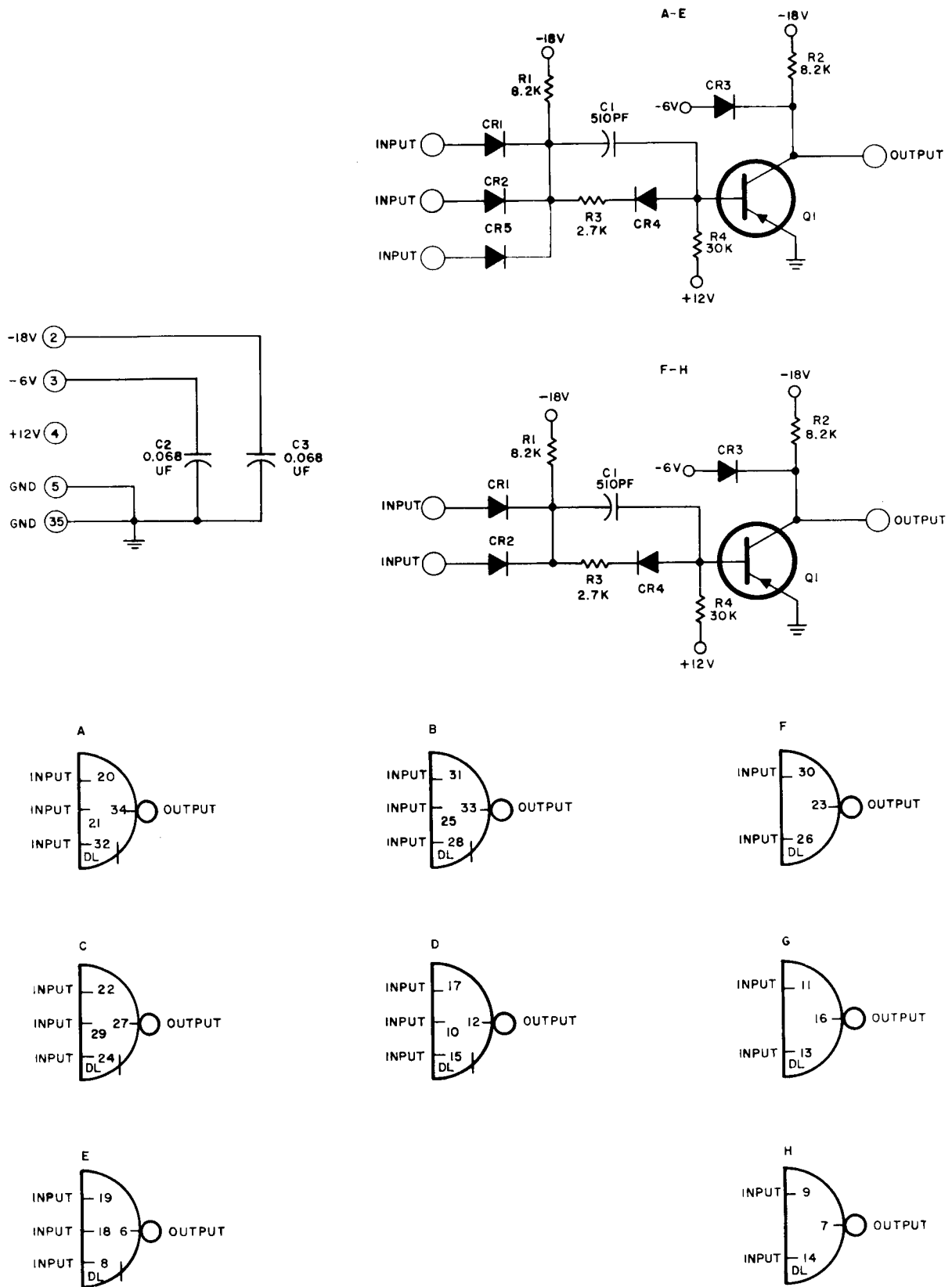


Figure 3-9A.3. NAND PAC, Model DL-20, Schematic Diagram

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3-10 DELAY MULTIVIBRATOR/PULSE SHAPER PAC, MODEL DM-20

GENERAL DESCRIPTION. Delay Multivibrator/Pulse Shaper PAC, model DM-20 (Figures 3-10.1 and 3-10.2), contains three independent and identical one-shot multivibrators capable of generating pulses in a variety of widths. The capacitors provided with each circuit may be wired for pulses of 3 to 200 μ sec in width. Externally connected capacitors can be used to obtain pulse widths up to several seconds. Each multivibrator has available a trigger input, an input node, and assertion and negation outputs. Each output is capable of driving four unit loads. The DM-20 is useful in applications requiring delayed levels or pulse shaping and standardizing.

CIRCUIT FUNCTION. Each DM-20 circuit (Figure 3-10.3) consists of a single input gate (expandable to 10 inputs via the input node) which is AC-coupled to a monostable multivibrator. A delay cycle is initiated by a positive-going transition at the input. The triggering input must stay positive at least 1.5 μ sec and must be negative at least 2.5 μ sec prior to the triggering action.

Pulse width, controlled by precision resistors, stable mica and film capacitors, and a Zener diode reference element, is essentially independent of temperature, power supply variations, ripple, etc. The required recovery period for the delay multivibrator is less than 80 percent of the pulse width, and begins immediately at the end of the delay period, regardless of the state of the input signal. The delay multivibrator can be triggered during the 50 to 80 percent of pulse width portion of the recovery period but yields a narrower than normal output signal. (See diagram, Typical DM-20 Recovery Curve.) The delay multivibrator should not be triggered during the recovery period from 0 to 50 percent of the pulse width. For example, if successive 10- μ sec delays are required, the time between triggering should not be less than 18 μ sec. Retriggering during the active pulse time does not affect circuit operation or cause any additional output.

Pulse width is controlled by connecting the appropriate capacitors to the delay node as indicated on the schematic. Two or more of the internally provided capacitors may be connected simultaneously and the resulting pulse has a width equal to the sum of the pulse widths indicated on the block

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diagram. For other delays, external capacitors should be connected across the delay and external delay node (terminals 7 and 8, 16 and 11, or 27 and 18, depending on which of the three circuits is used. The value of the external capacitor is calculated from the equation $C = 340 (PW - 2.5 \mu\text{sec})$, where C is capacitance in picofarads and PW is pulse width in μsec .

TABLE 3-10.1.
DELAY MULTIVIBRATOR OUTPUT DELAY WIDTHS AND PROPER
JUMPER CONNECTIONS AT THE PAC CONNECTOR

Delay Width	Jumper Connections		
	Circuit A	Circuit B	Circuit C
3 μsec	None required	None required	None required
9 μsec	Pins 12 and 8	Pins 20 and 11	Pins 32 and 18
20 μsec	Pins 13 and 8	Pins 21 and 11	Pins 33 and 18
45 μsec	Pins 14 and 8	Pins 24 and 11	Pins 34 and 18
200 μsec	Pins 15 and 8	Pins 23 and 11	Pins 35 and 18
For all other delay widths	Connect an external capacitor between pins 7 and 8	Connect an external capacitor between pins 16 and 11	Connect an external capacitor between pins 27 and 18

SPECIFICATIONS.

Input Loading

2 unit loads

Circuit Delay

1.2 μsec (max) negation output
0.6 μsec (typ) negation output
0.8 μsec (max) assertion output
0.4 μsec (typ) assertion output

Width Accuracy

$\pm 10\%$ from circuit to circuit
(2 % on special order)

Frequency of Operation

DC to $(\frac{1}{1.8 \times PW})$ or 100 KC,
whichever is less, where PW is pulse width in μsec .

Internally Provided Pulse Widths

3 μsec , 9 μsec , 20 μsec , 45 μsec ,
and 200 μsec

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Pulse Width Variations (all independently specified)

Short-term stability (8 hours)	<1%
Jitter (pulse-to-pulse)	<0.1%
Long-term stability (reproducibility over 3 months)	<2%
Temperature variation (-20°C to +55°C)	<2%

Recovery Time

80% of pulse width (Figure 3-10.4) (See DM-2 Recovery Curve)

Output Waveform Characteristics

Assertion Output (negative pulse measured from -0.6 V to -4.5 V)

Rise time: 1.0 μ sec or 0.2 percent of pulse width, whichever is longer

Fall time: 0.8 μ sec (typ)

NOTE

A positive-going edge, adequate for triggering of another DM-20, is assured on trailing edge of assertion pulses up to 1 msec wide. For wider pulses (longer delays), inversion of the negation output is recommended for triggering of AC inputs and DM-20s.

Negation Output (positive pulse)

Rise time: 0.5 μ sec (typ)

Fall time: 0.8 μ sec (typ)

Output Drive Capability

4 unit loads

Total Power

1.0 W

Current Requirements

-18 V: 55 ma

-6 V: 13 ma (reverse current into supply)

+12 V: 1.3 ma

Polarization

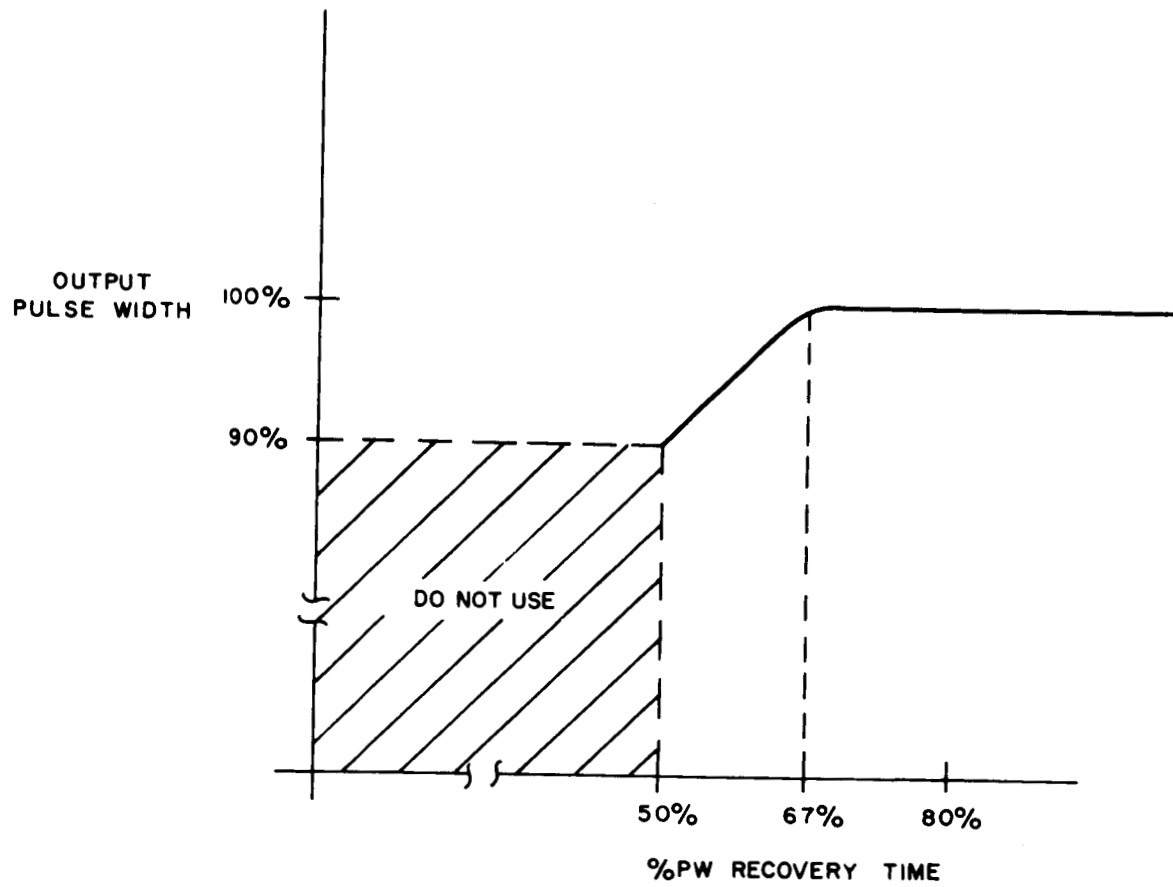
Pins 18 and 20

Handle Color Code

Long: Yellow

Short: Yellow

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Typical DM-20 Recovery Curve

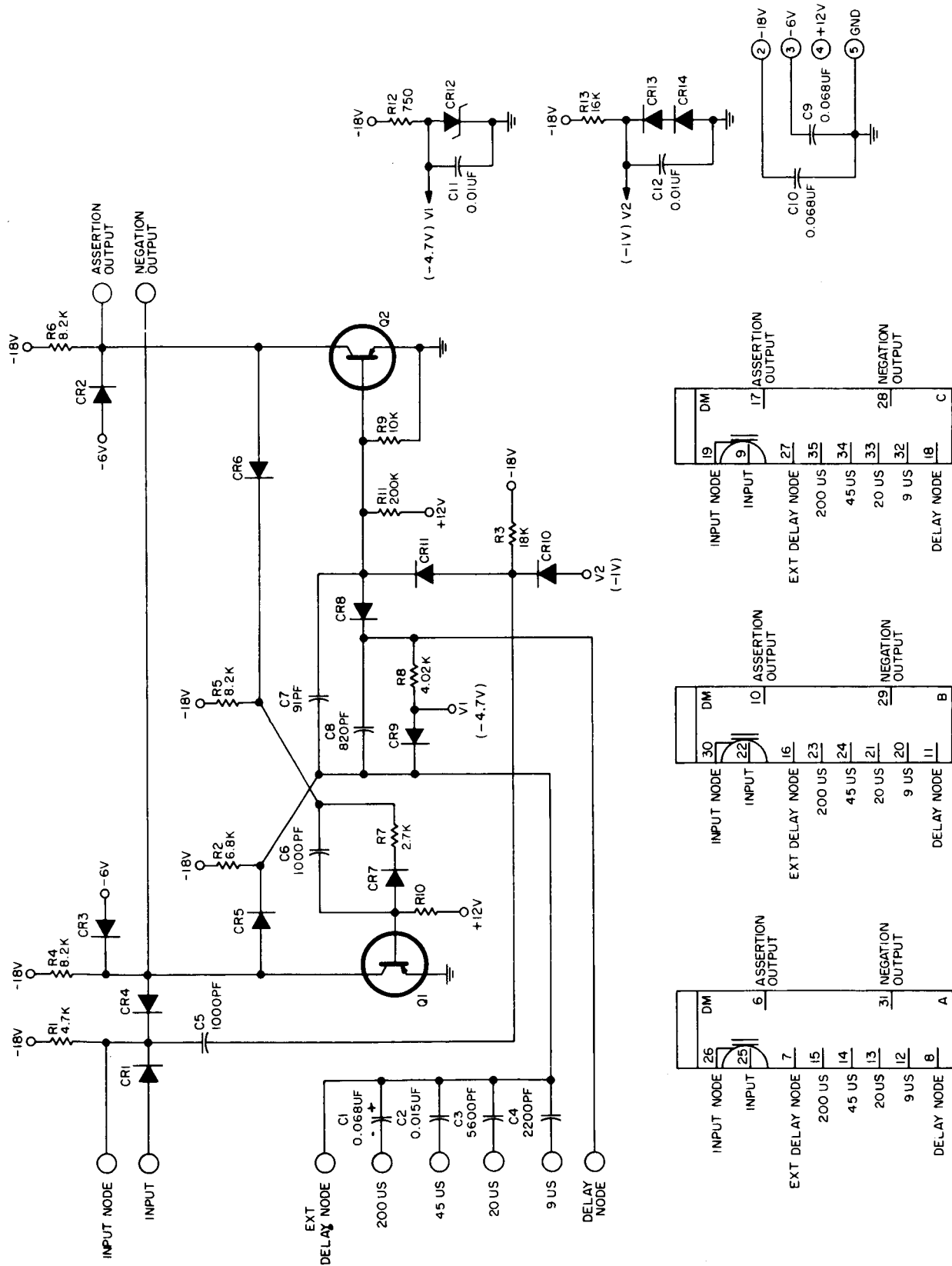


Figure 3-10.3. Delay Multivibrator Pulse Shaper PAC, DM-20, Schematic and Block Diagram

3-13

DELAYED PULSE PAC, MODEL DS-20

GENERAL DESCRIPTION. Delayed Pulse PAC, model DS-20, (Figure 3-13.1) contains two monostable multivibrators that generate delays in a variety of widths, and two pulse shaper circuits. Each monostable multivibrator drives a pulse shaper that delivers a pulse at the end of the delay. Hence, the PAC provides pulses delayed relative to an input signal, and performs pulse shaping and standardization functions. Each pulse shaper has two inputs: one is internally connected to the assertion output of an associated multivibrator; the other, in conjunction with the multivibrator output, can be used to implement various logic forms for delaying and timing applications.

The monostable multivibrator provides both assertion and negation delay pulse widths of 3, 9, 20, 45, or 200 μsec . Other delay widths can be obtained through use of external components.

The pulse shaper provides a 3- μsec assertion pulse. Wider pulse widths can be obtained through use of external components. In normal operation, the pulse shaper circuit is triggered on the trailing edge of the delay multivibrator assertion output signal, thus providing a pulse at the end of the delay.

CIRCUIT FUNCTION. There are two independent and identical pairs of circuits on the DS-20 PAC (Figure 3-13.2). Each pair, identified as circuit A and circuit B, consists of a delay multivibrator driving a pulse shaper. This discussion is limited to circuit A.

Delay Multivibrator. Each delay multivibrator circuit contains a single AC input plus a node for expanding to 10 inputs. A positive-going transition at the input triggers the multivibrator. The triggering input must have a rise time no greater than 1.0 μsec and all inputs must be negative at least 2.5 μsec prior to the triggering action.

Delay pulse width is controlled by precision resistors, stable mica and film capacitors, and a zener diode. The delay width is essentially independent of temperature, power supply variations, and ripple.

The required recovery period for the multivibrator is less than 80 percent of the delay width and begins immediately at the completion of the delay period regardless of the state of the input signal. The multivibrator

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can be triggered during the 50 to 80 percent delay width portion of the recovery period (Figure 3-13.3) but yields a narrower than normal output signal. The multivibrator should not be triggered during the 0 to 50 percent delay width portion of the recovery period. For example, if successive 10- μ sec delays are required, the time between triggering should not be less than 18 μ sec. Retriggering during the active delay time does not affect circuit operation.

The circuit provides for the selection of five fixed delays; 3, 9, 20, 45, and 200 μ sec. The output delay width is controlled by connecting the appropriate PAC connector pins as outlined in Table 3-13.1. These conditions essentially parallel capacitors. Other delays can be obtained by connecting an external capacitor to the PAC connector as indicated in Table 3-13.1.

TABLE 3-13.1
DELAY MULTIVIBRATOR OUTPUT DELAY WIDTHS AND PROPER
JUMPER CONNECTIONS AT THE PAC CONNECTOR

Delay Widths	Jumper Connections	
	Circuit A	Circuit B
3 μ sec	None required	None required
9 μ sec	Pins 19 and 12	Pins 32 and 17
20 μ sec	Pins 21 and 12	Pins 33 and 17
45 μ sec	Pins 22 and 12	Pins 34 and 17
200.0 μ sec	Pins 23 and 12	Pins 35 and 17
For all other delay widths	Connect an external capacitor between pins 15 and 12*	Connect an external capacitor between pins 25 and 17*

*The value of the external capacitor can be calculated from the equation:
 $C = 340 (DW - 2.5)$ where DW is the delay width in μ sec, and C is the capacitance in picofarads (pf).

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Pulse Shaper. The pulse shaper circuit is an AC-coupled inverter that provides a standard 3 μ sec assertion pulse output. The circuit is triggered on the positive transition of the input signal and the pulse width is determined by an RC network. The pulse width can be increased by adding a parallel capacitor to the capacitor provided on the PAC as shown in Table 3-13.2. The value of the parallel capacitor required for a specific output pulse width can be calculated from the equation: $C = (PW - 2.5) \times 0.8 \times 10^3$ where PW is the pulse width in μ sec and C is the capacitance in picofarads (pf). The parallel capacitor can be added in two ways: installed in a space provided on the PAC referred to as CX, or externally connected to the PAC connector (refer to Table 3-13.2 for connections and Figure 3-13.4).

TABLE 3-13.2.
PULSE SHAPER, JUMPER CONNECTIONS AT THE
PAC CONNECTOR TO CHANGE PULSE WIDTH

Method	Jumper Connections	
	Circuit A	Circuit B
Add parallel capacitors in space marked CX	Pins 10 and 8	Pins 24 and 29
Add external capacitors	Connect capacitor between pins 6 and 8	Connect capacitor between pins 31 and 29.

Both inputs to the pulse shaper must conform to these general rules:

- a. The input waveform must be positive for a time equal to or greater than the required output pulse width.
- b. The input waveform must be negative, prior to going positive, for a time equal to or greater than the desired output pulse width.

As these rules imply, minimal cases require that the input waveform be symmetrical. Examples of the input waveforms required are shown in Figure 3-13.5a and b.

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The input leads to the pulse shaper input circuit should be as short as possible to prevent noise and spurious transients.

In normal operation the pulse shaper circuit is triggered on the trailing edge of the delay multivibrator assertion output signal, thus providing a pulse at the end of a delay.

In most applications, the available input to the pulse shaper is used to inhibit the circuit (Figure 3-13.5c) That is, an applied logic ZERO (0 V) at the available input prevents triggering of the pulse shaper. The additional pulse shaper input may be used to generate output pulses during the active delay period (Figure 3-13.5d).

SPECIFICATIONS.

Multivibrator Specifications

Input Loading

2 unit loads each

Frequency of Operation

DC to $\left(\frac{1}{1.8 \times DW}\right)$ or 100 KC,
whichever is less, where
DW is delay
width in μsec .

Circuit Delay

Negation Output: 1.2 μsec (max)

0.6 μsec (typ)

Assertion Output: 0.8 μsec (max)

0.4 μsec (typ)

Output Drive Capability

Assertion: 2 unit loads each

Negation: 4 unit loads each

Output Waveform Characteristics

Assertion Output (negative pulse measured from -0.6 V to -4.5 V)

Rise time: 1.0 μsec or 0.2 percent of pulse width, whichever is longer

Fall time: 0.8 μsec (typ)

NOTE

A positive-going edge, adequate for triggering of other DS-20s, is assured on trailing edge of assertion up to 1 msec wide. For wider pulses (longer delays), inversion of the negation output is recommended for triggering of AC inputs and other DS-20s.

Negation Output (positive pulse)

Rise time: 0.5 μsec (typ)

Fall time: 0.8 μsec (typ)

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Delay Width Specifications

Internally provided delay widths: 3, 9, 20, 45, and 200 μsec

Delay width accuracy: $\pm 10\%$ (2% on special order)

Delay width variations (all independently specified):

Short term stability (8 hours)	<1%
Jitter (delay to delay)	<0.1%
Long term stability (reproducibility over three months)	<2%
Temperature variation (-20°C to +55°C)	<2%

Recovery time: 80% of the delay width (Figure 3-13.3)

Pulse Shaper Specifications

Standard Output Pulse Width

3 μsec

Input Loading

3 unit loads each

Output Waveform Characteristics

Rise time: 0.5 μsec (typ)

Fall time: 0.8 μsec (typ)

Output Drive Capability

Assertion: 5 unit loads and
100 pf stray capacitance each output

Pulse Width (max)

Limited only by the general rules listed in Table 3-13.2.

Handle Color Code

Long: Yellow

Short: Green

Current Requirements

-18 V: 70 ma

- 6 V: 12 ma (reverse current into supply)

+12 V: 12 ma

Polarization

Pins 14 and 32

Total Power

1.4 W



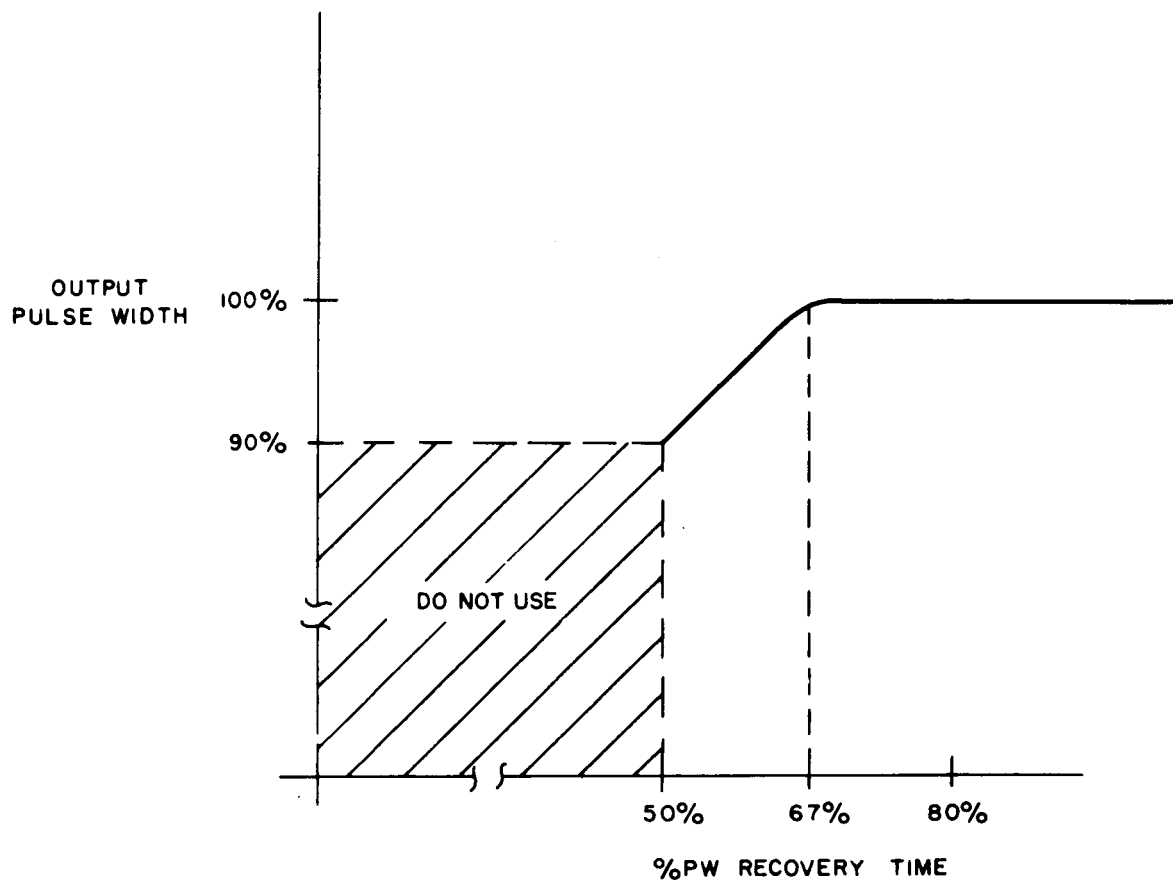


Figure 3-13.3. Typical Delay Multivibrator Recovery Curve

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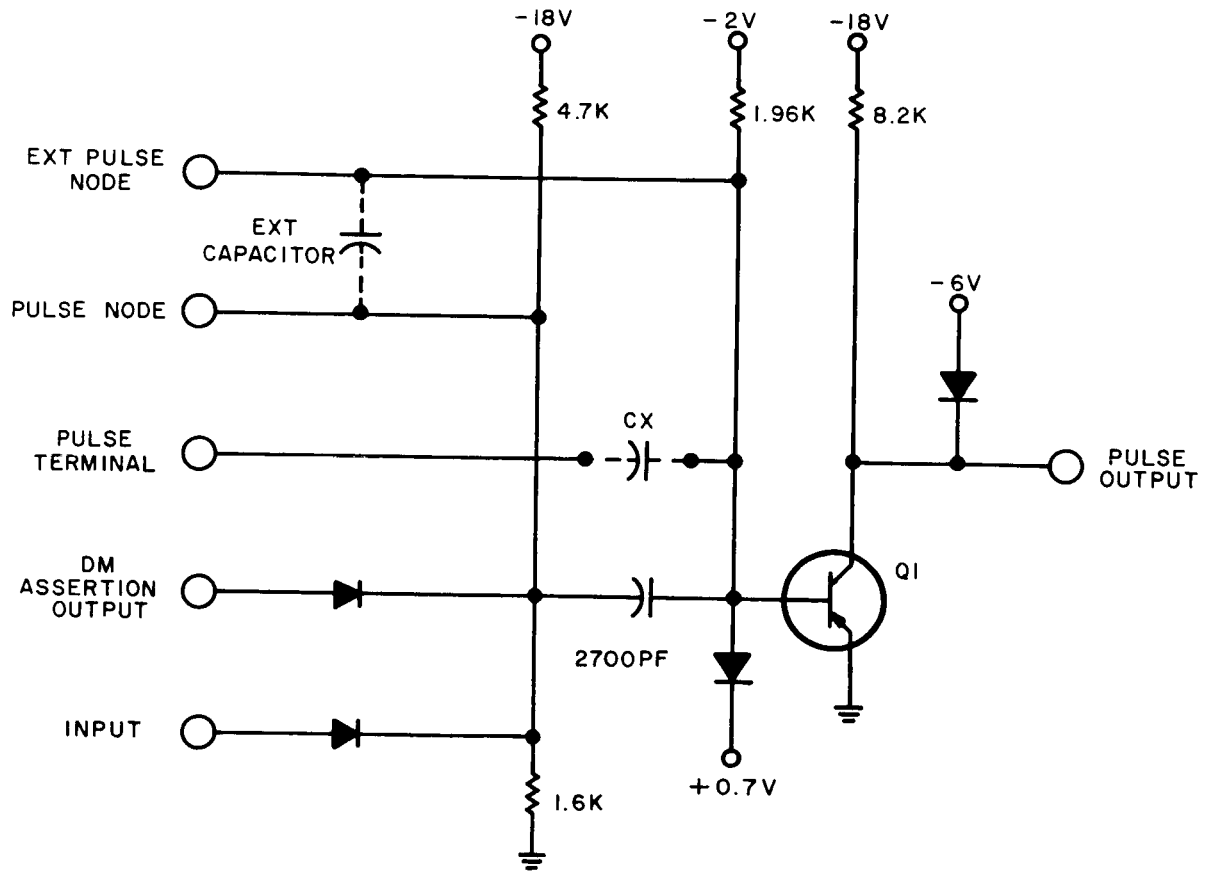
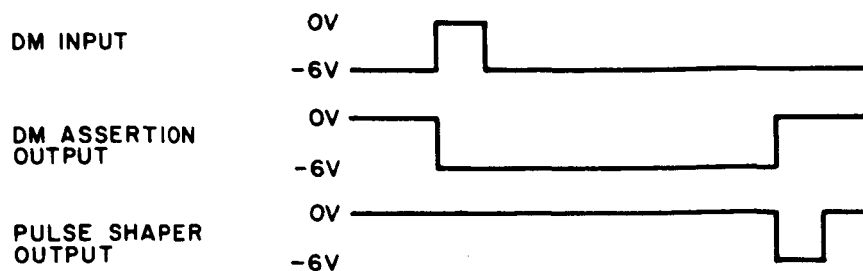


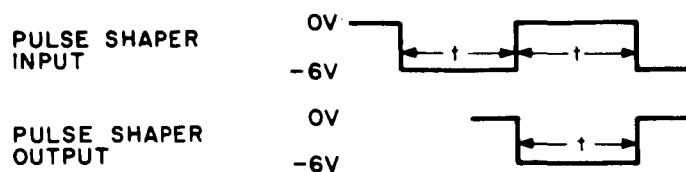
Figure 3-13.4. Pulse Shaper Using External Capacitor

8/31/62

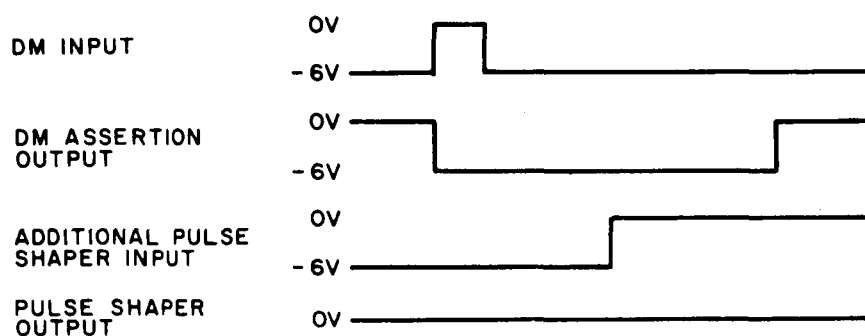
200-KC S-PAC DIGITAL MODULES



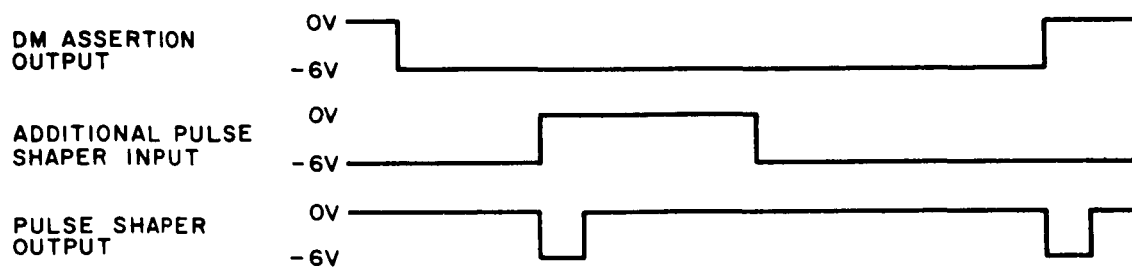
a. Normal Operation



b. Minimum Input For An Output Pulse Width t



c. Using Additional Pulse Shaper Input To Inhibit Pulse Shaper



d. Using Additional Pulse Shaper Input To Generate Output Pulses

Figure 3-13.5. DS-20 Waveforms

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3-15

GATED FLIP-FLOP PAC, MODEL FA-20

GENERAL DESCRIPTION. The AC gated flip-flop PAC, model FA-20 (Figures 3-15.1 and 3-15.2), contains four identical, independent bistable circuits that respond to transitional input signals, and can be wired to perform any logic function required of a flip-flop, such as counting, shifting, accumulating, etc. Each stage has three independent AC coupled inputs: consisting of a reset input and two set inputs. Level control inputs are provided with the AC reset input and one of the AC set inputs to allow gating of set and reset information. The AC set and reset inputs can be wired separately in applications calling for independent setting and resetting of the flip-flop. The inputs can also be tied together to implement logic functions such as shifting, complementing, parallel information drop-in, etc. These applications are detailed in paragraph a. A DC reset input, common to the four flip-flop circuits, is provided to permit simultaneous clearing of all four stages.

CIRCUIT FUNCTION. The four FA-20 circuits are identical. Each stage consists of two cross-coupled NAND gates with AC-coupled inputs (Figure 3-15.3).

a. AC Set (Reset) Input and Level Control (see paragraph 2-10). The AC set (reset) input and associated level control form a two-input AC gate which, when properly activated, causes the flip-flop to assume the set (reset) state. Proper activation of the gate requires that the level control be a ZERO (0 V) and a positive-going 6-volt step be applied to the AC input (paragraph b). The 6-volt step is differentiated and applied to the flip-flop input through a biased diode. If the level control is a ONE (-6 V), the differentiated step is blocked. The additional AC set input also forms a two-input AC gate with the level control internally wired to the set output. The flip-flop is unconditionally set every time a positive-going 6-volt step is applied to this AC set input.

b. Timing. There are two modes of operation for AC inputs with level controls. The first is pulse mode of operation, which is defined as the condition where the level control signal switches negative when the AC input signal is positive. The required AC input signal for this mode of operation is a negative pulse of 2.5 μ sec minimum pulse width.

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The second mode of operation is the step mode, which is defined as the condition where the level control switches negative when the AC input signal is negative. This mode requires that the AC input signal remain negative 6 μ sec minimum after the level control switches negative. Figure 3-15.4 illustrates the waveforms associated with both modes of operation.

c. Shifting. Each stage of the FA-20 can be wired to perform the function of shifting. The AC reset inputs and the AC set inputs having the level control are connected to form the shift input. The level control inputs and the outputs of the four stages are then connected in a shift register configuration as illustrated in Figure 3-15.5. Input information to the register is applied to the level control inputs of the first stage and must conform to the specifications outlined in the timing description. The shift input is sensitive to positive-going 6-volt steps and incorporates trailing-edge triggering for negative shift pulses (Figure 3-15.6). This allows the output of the register to be gated with the shift signal without need for delay circuits or two-phase clocks.

d. Complementing. Each stage of the FA-20 may be wired to perform the function of complementing. This is accomplished by connecting the AC reset input to either of the two AC set inputs, thus forming the complement input. The reset level control is connected to the reset output. If the AC set input having the level control is used to form the complement input, the set level control must be connected to the set output. However, if the other set input is used, no connection is required since its level control is internally wired to the set output. The complement input is sensitive to positive-going 6-volt steps. For trailing edge triggering of the flip-flop, negative signals of 2.5 μ sec minimum duration should be used. For leading edge triggering, positive signals of 1.5 μ sec minimum duration are required, with the additional requirement that the positive signals represent at most a 50 percent duty factor at 200 KC. Figure 3-17.7 shows the FA-20 wired as a binary counter with each stage performing the complementing function.

e. Parallel Information Drop-In. Each stage of the FA-20 can be wired to accept information in parallel with the advantages of built-in pulse dodging, and requiring no additional gating. Parallel information drop-in is accomplished by connecting the AC reset input to the AC set input having the level control. The combined inputs of each stage are then tied together to

200-KC S-PAC DIGITAL MODULES

form a common input. The input information should be in the form of complementary logic signals such as the outputs of any S-PAC flip-flop, and should be connected to the level control inputs. A level control input at ZERO causes the flip-flop to assume the state associated with that level control when the common input becomes positive, that is, the flip-flop becomes set if the set level control is 0 volt. If the input data is presented from the output of a gate (signal-ended), an inverter must be provided between the set and reset level control inputs.

The set and reset level controls should be connected to the reset and set outputs, respectively, of the driving flip-flop. Having both level controls at -6 volts or disconnected disables the common input. If both level controls are at ZERO when the common input becomes positive, the flip-flop is caused to assume an indeterminate state. Information is put into the FA-20 register on each positive transition of the common input signal. Figure 3-15.8 illustrates the FA-20 wired to accept information in parallel. Refer to the timing description (subparagraph 3-15b) for input waveform requirements.

NOTE

For all applications of the FA-20, pin 35 should be jumpered to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

200 KC S-PAC DIGITAL MODULES

SPECIFICATIONS

Input Loading

AC set or reset inputs: 2 unit loads each used separately
Level control input: 1/2 unit load each
Common (DC) reset input: 4 unit loads

Circuit Delay (measured at -3 V)

0.6 μ sec (typ) reset input to set output or set input to reset output
1.2 μ sec (max)
0.4 μ sec (typ) set input to set output or reset input to reset output
0.8 μ sec (max)

Frequency of Operation

DC to 200 KC (max)

Output Drive Capability

6 unit loads and 500 pf stray capacitance each

Total Power

1.6 W

Polarization

Pins 4 and 32

Output Waveform Characteristics

Rise time: 0.5 μ sec (typ)

Fall time: 0.8 μ sec (typ)

Current Requirements

-18 V: 86 ma

- 6 V: 42 ma (reverse current into supply)

+12 V: 3.5 ma

Handle Color Code

Long: Blue

Short: Brown

200-KC S-PAC DIGITAL MODULES

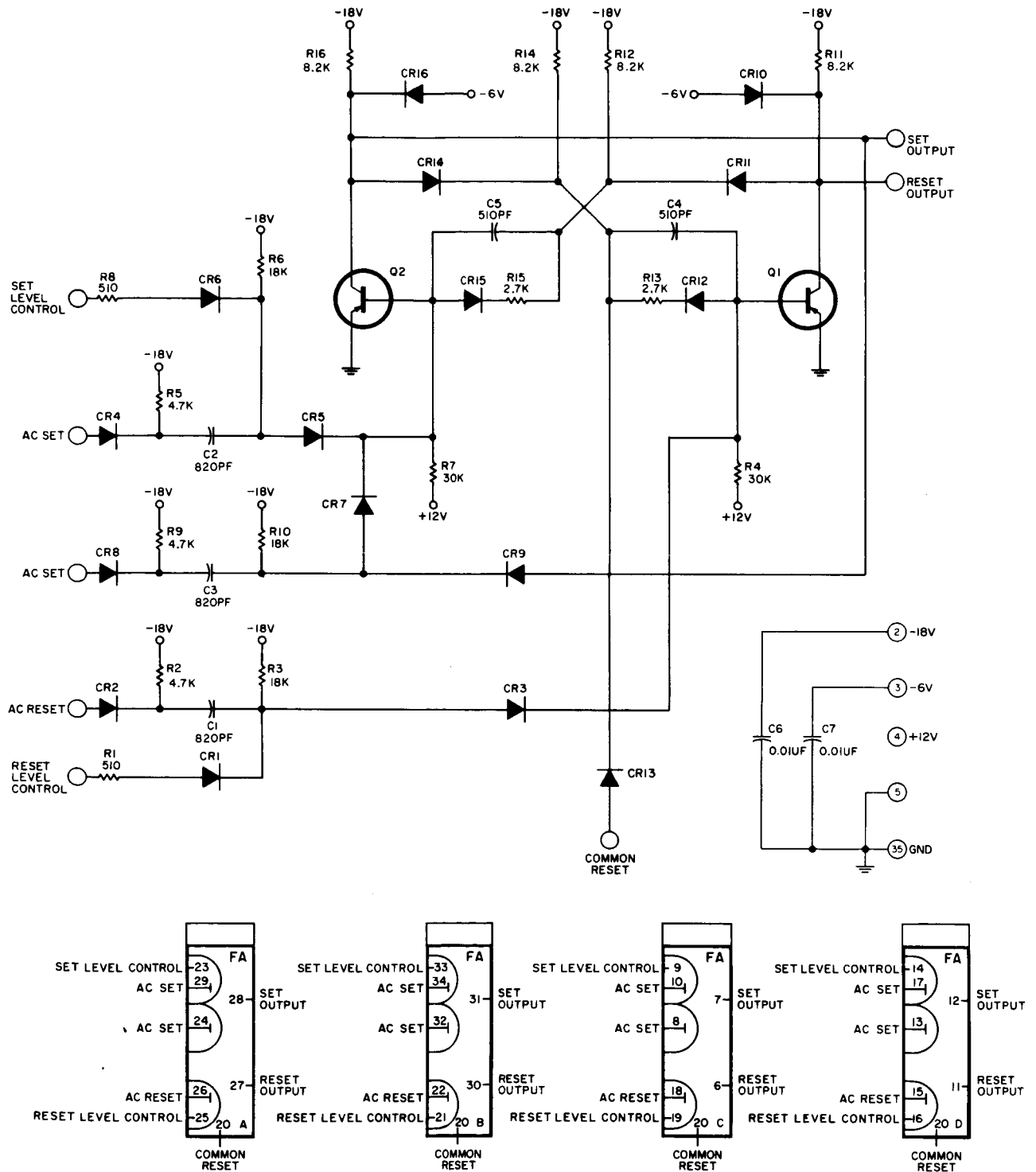


Figure 3-15.3. Gated Flip-Flop PAC, FA-20, Schematic and Block Diagram

200-KC S-PAC DIGITAL MODULES

3-16

BASIC FLIP-FLOP PAC, MODEL FF-20

GENERAL DESCRIPTION. Basic Flip-Flop PAC, model FF-20 (Figures 3-16.1 and 3-16.2), contains four identical, independent, bistable circuits for use as input-output registers or for any logic application in which complementing, shifting, etc., is not required. One DC set and two DC reset inputs are provided. Each input is expandable to ten by connecting diode clusters to the appropriate node.

CIRCUIT FUNCTION. The basic flip-flop circuit (Figure 3-16.3) consists of two cross-coupled NAND gates. When all DC inputs are at ONE (-6 V), the flip-flop assumes one of its bistable states. Applying ZERO (0 V) to a DC set or reset input for 1.5 μ sec or longer causes the flip-flop to assume the set or reset stage respectively, unless already in that state. The flip-flop can be both set and reset in a 5- μ sec interval.

If both set and reset DC inputs are held at ZERO, a third state exists in which both set and reset outputs are at ONE.

NOTE

In all applications of the FF-20, pin 35 should be jumpered to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

200-KC S-PAC DIGITAL MODULES

SPECIFICATIONS.

Input Loading

1 unit load each

Frequency of Operation

DC to 200 KC (max)

Circuit Delay (measured at -3 V)

0.6 μ sec (typ) reset input to set output or set input to reset output

1.2 μ sec (max)

0.4 μ sec (typ) set input to set output or reset input to reset output

0.8 μ sec (max)

Output Waveform Characteristics

Rise Time: 0.5 μ sec (typ)

Fall Time: 0.8 μ sec (typ)

Current Requirements

-18 V: 32 ma

- 6 V: 8 ma (reverse current
into supply)

Output Drive Capability

6 unit loads plus 500 pf stray
capacitance each

+12 V: 3.5 ma

Polarization

Pins 16 and 18

Total Power

0.6 W

Handle Color Code

Long: Blue

Short: Blue

200-KC S-PAC DIGITAL MODULES

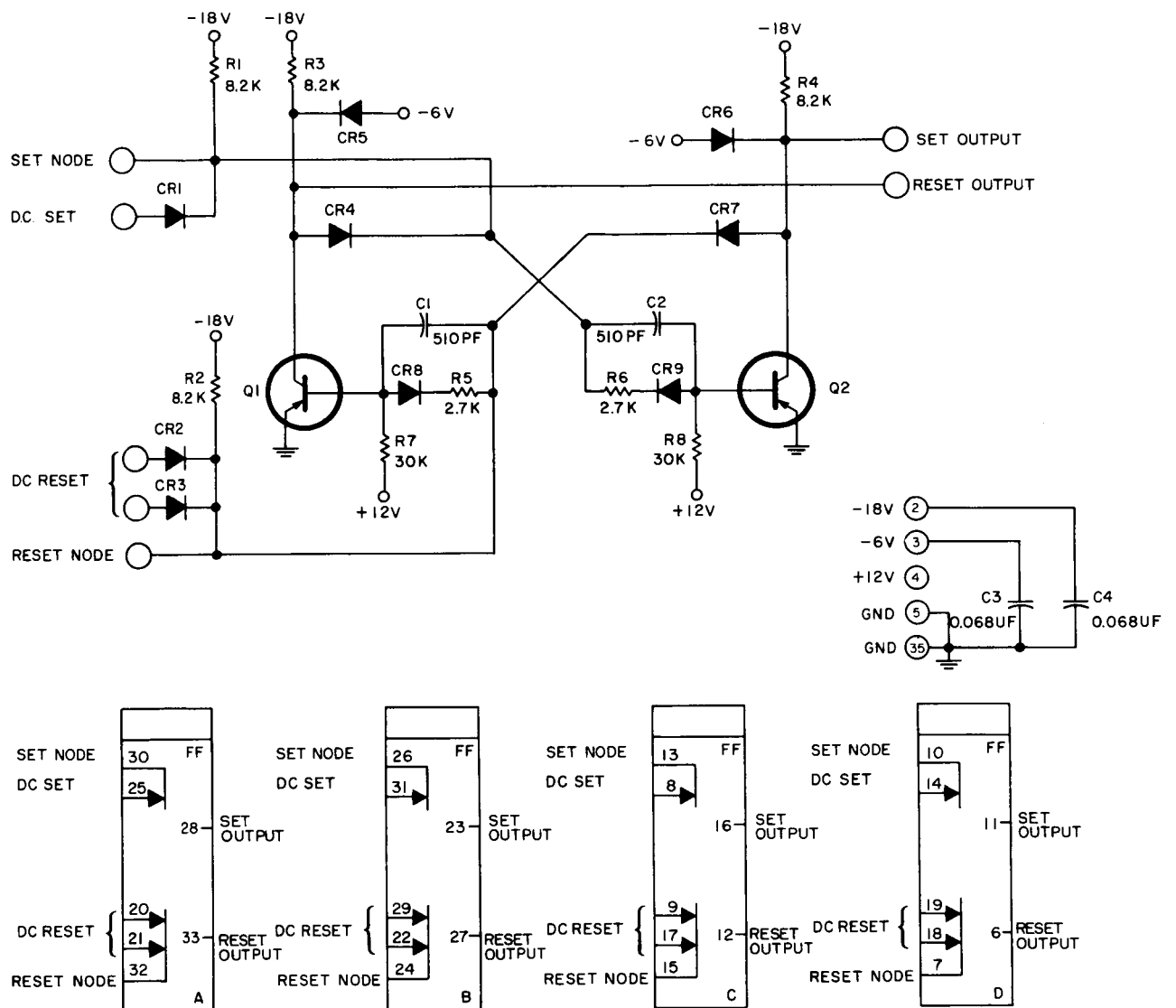


Figure 3-16.3. Basic Flip Flop PAC, FF-20, Schematic and Block Diagram

200-KC S-PAC DIGITAL MODULES

3-18

LAMP DRIVER, MODEL LD-30

GENERAL DESCRIPTION. Lamp Driver, model LD-30 (see Figure 3-18. 1), contains 14 identical and independent transistor-driver circuits for use with external indicator lamps. The circuit operates from standard S-PAC levels. Each circuit can deliver 70 milliamperes to an indicator lamp with a rated operating voltage between -6 and -24 volts.

The -18 volts from a standard S-PAC power supply can drive any lamp rated from -18 to -28 volts. The use of a 28-volt bulb at 18 volts provides durability and low power consumption with adequate illumination for most applications.

CIRCUIT FUNCTION. The lamp is connected in series between the collector of the transistor and the negative supply voltage (Figure 3-18. 2). When the input to the circuit is a ONE (-6 V), or an open circuit, the transistor turns on and the lamp illuminates. When the input is a ZERO (0 V), the transistor is biased off and the lamp extinguishes.

NOTE

The negative supply voltage return should be connected to pin 35 on this PAC.

SPECIFICATIONS.

Input Loading

1 unit load each

Current Requirements

(assuming all circuits are used)

-18 V: 84 ma (max)

+12 V: 16 ma

Polarization

Pins 18 and 30

Output Drive Capability

70 ma at any lamp supply
voltage between -6 V and
-24 V

Total Power

(assuming all circuits are used)
1.7 W

Handle Color Code

Long: Brown

Short: Red

200-KC S-PAC DIGITAL MODULES

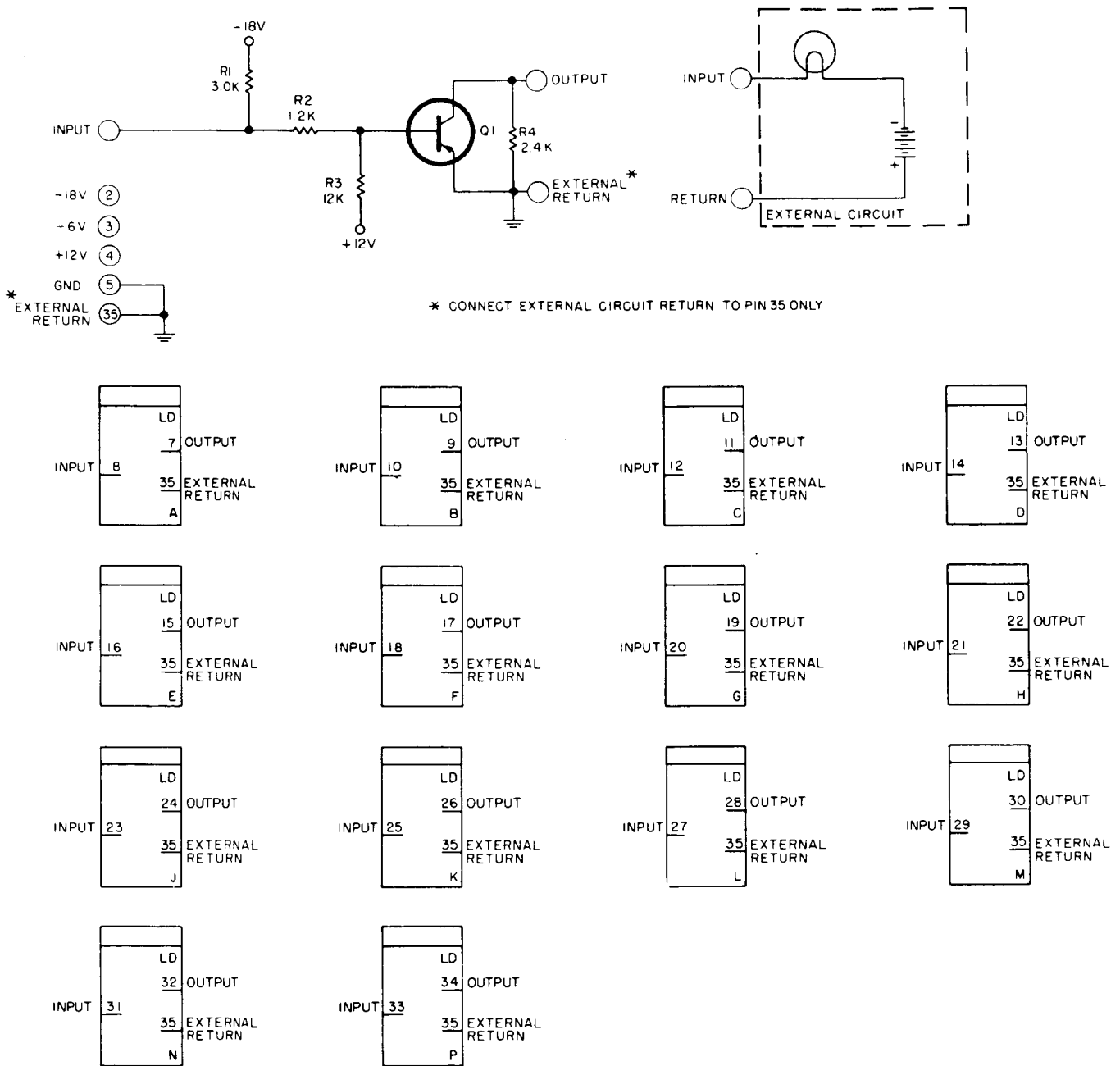


Figure 3-18.2. Lamp Driver PAC, LD-30, Schematic and Block Diagram

200-KC S-PAC DIGITAL MODULES

3-28 POWER SUPPLIES, MODELS RP-30, RP-31, and RP-32

GENERAL DESCRIPTION. The S-PAC Power Supplies, models RP-30, RP-31, and RP-32 (Figure 3-28.1, 3-28.4, and 3-28.7) are integrally packaged, regulated power sources containing the three S-PAC voltages with proportioned current capability.

They are substantially derated at rated load and may safely be operated at full load over their specified environmental temperature range. In specific cases, it may also be possible to operate a supply slightly beyond its ratings when used in an air-conditioned laboratory environment. The supplies employ ferroresonant transformers to minimize the effects of line voltage variations and use high-gain, solid-state regulator circuits to achieve the excellent ripple, regulation, and stability specified.

The supplies are stacked so that no special provision need be made for the reverse current on the -6 volt of the S-PACs. The power supply schematics are shown in Figures 3-28.3, and 3-28.6, and 3-28.9.

200-KC S-PAC DIGITAL MODULES

RP-30, RP-31, AND RP-32 SPECIFICATIONS.

Input Power Requirements

Input Voltage: 105 to 125 V RMS

Frequency: 58 to 62 CPS, single phase (400-cycle on special order)

Output

Voltage and Load Current:

Model RP-30	-18 VDC: 0 to 2 amp
	- 6 V: 0 to 2 amp
	+12 VDC: 0 to 0.8 amp
Model RP-31	-18 VDC: 0 to 8 amp
	- 6 V: 0 to 8 amp
	+12 VDC: 0 to 1.6 amp
Model RP-32	-18 VDC: 0 to 20 amp
	- 6 V: 0 to 20 amp
	+12 VDC: 0 to 3 amp

200-KC S-PAC DIGITAL MODULES

The following specifications apply to all supplies.

Regulation

Better than 0.75% for load (0 to maximum) and line voltage change

Stability

0.03% / °C from 10°C to 50°C

Ripple

Less than 75 MV PP at full load

Source Impedance

Consistent with regulation, $Z = \frac{\Delta e}{I_L}$

Ambient Temperature

Rated operation is from -10°C to 50°C at full load. All semi-conductors are rated not to exceed junction temperature of 80°C at full load and maximum ambient temperature.

Size

RP-30	5-1/4" H x 13" D x 19" W, relay rack mounting
RP-31	5-1/4" H x 15" D x 19" W, relay rack mounting
RP-32	8-3/4" H x 15" D x 19" W, relay rack mounting

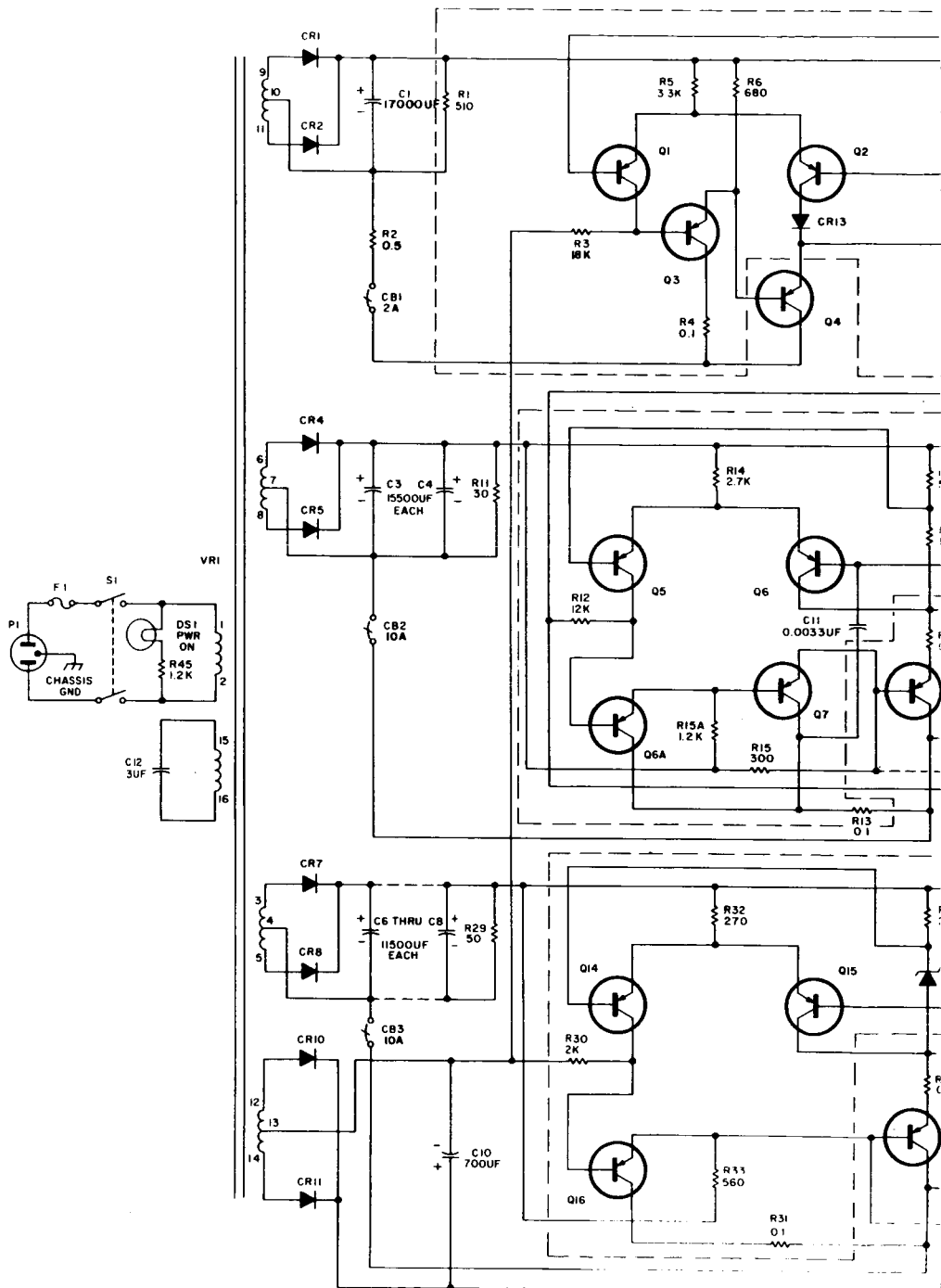
Weight

RP-30	30 lbs
RP-31	45 lbs
RP-32	90 lbs

200-KC S-PAC DIGITAL MODULES

General

1. AC and DC power-on indicators are provided.
2. DC outputs are protected by fast acting circuit breakers and an indicator is provided to indicate DC power failure.
3. All supplies are factory preset. Screwdriver adjustment is provided for recalibration if necessary. (Range of adjustment 2 percent)
4. Provision is made for one output terminal on each supply per 2-ampere rating of -18-volt supply. This allows individual power wiring to each S-BLOC, if desired.
5. Supplies are floating with respect to chassis. Chassis ground terminal is provided.



8/31/62

53-1

200-KC S-PAC DIGITAL MODULES

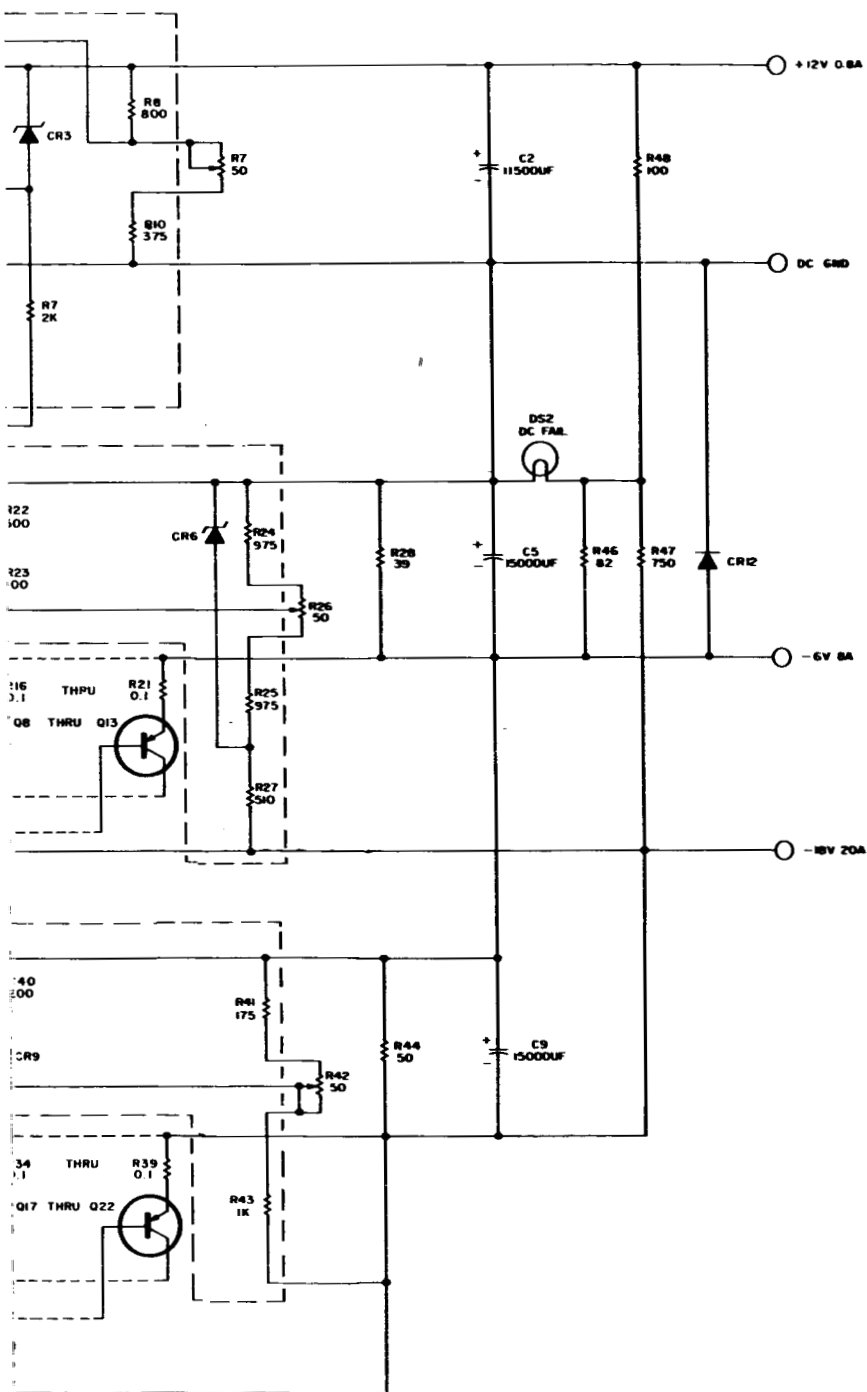
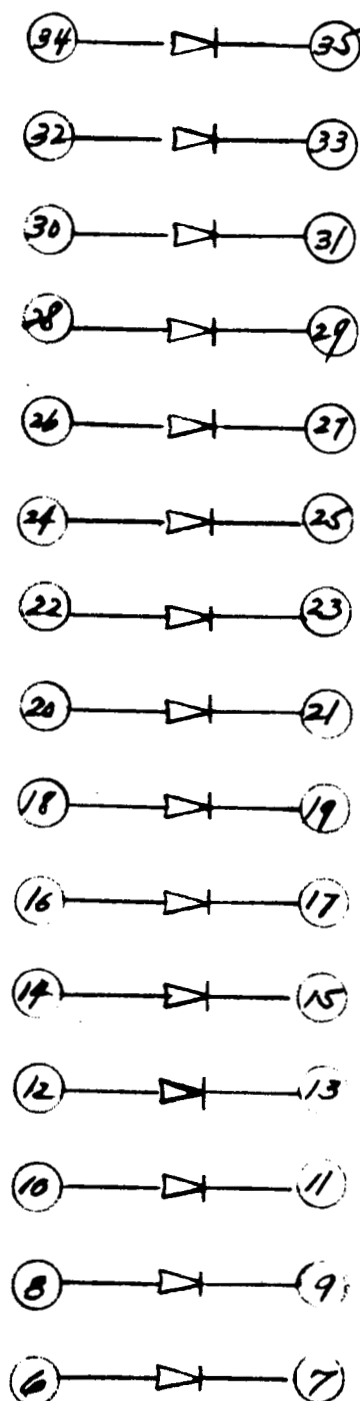


Figure 3-28. 6. Power Supply, RP-31, Schematic Diagram

C-53.7

SPECIAL DIODE BOARD - BPX



ARACON
9G8-20E

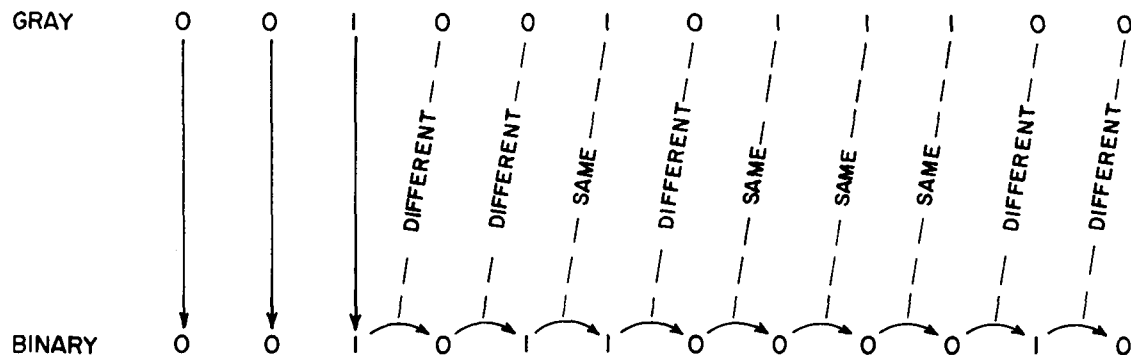
APPENDIX D DECIMAL LISTING OF GRAY CODE NUMBERS FROM PAPER TAPE

Many of the system checks listed in Section 4 require readings from the shaft encoders. The output of the shaft encoders is a 12-bit gray-coded binary number, divided into two six-bit frames on paper tape (punch levels 2^5 through 2^0) with the upper six bits preceding the lower six. The gray codes may be converted to decimal numbers by hand or by the 160-A with the use of a special gray code to decimal conversion routine.

D.1 Manual Conversion

1. List the gray-code numbers from the paper tape. A hole corresponds to a ONE.
2. Change a gray-code number to binary as follows:
 - (a) Any initial ZEROS and also the first ONE remain as in gray code.
 - (b) Inspect the next (Nth) gray-code digit. If it is a ONE, the Nth binary digit should be the opposite of the preceding binary digit. If, on the other hand, the Nth gray-code digit were a ZERO, the Nth binary digit should be made the same as the preceding binary digit.

EXAMPLE:



- (c) Convert pure binary numbers to decimal numbers through the use of (1) a binary to decimal conversion table or (2) an intermediate conversion to octal numbers, followed by an octal to decimal conversion. The conversion to octal is readily accomplished by arranging the binary bits in groups of three as shown in the following example.

Pure Binary	0 1 0	0 0 1	1 0 1	1 0 1
Octal	2(8 ³)	1(8 ²)	5(8 ¹)	5(8 ⁰)

If no octal to decimal conversion table is available, the final conversion to decimal may be accomplished by multiplying the digits by eight raised to the power corresponding to digit position and obtaining the sum. The number of the previous example is converted as follows:

$$\begin{array}{rcl}
 2 \times 8^3 \text{ or } 512 & = & 1024 \\
 1 \times 8^2 \text{ or } 64 & = & 64 \\
 5 \times 8^1 \text{ or } 8 & = & 40 \\
 5 \times 8^0 \text{ or } 1 & = & 5 \\
 \hline
 1133_{10} & = & 2155_8
 \end{array}$$

D.2 Computer Conversion

When preparing a paper tape with film-reader measurements, an END code must precede and follow the shaft encoder gray code punches. Several blocks of measurements can be separated (on computer output) by interspersing two END codes between blocks. For example: END, data block, END, END data block END.

After preparation of the data tape, obtain a paper tape copy of the gray-to-binary printer routine and:

1. Master clear 160-A
2. Turn on paper tape reader and position the converter-routine tape in the reader.
3. Set the LOAD-CLEAR switch to LOAD.

4. Set the RUN-STEP switch to RUN.
The paper tape will load and the computer will stop.
5. Turn on line printer, change paper tape guide and level switch to 8-level and insert film reader tape.
6. Master clear and run. The first block of data (between two END codes) will be printed in the sequence in which it is punched on tape. Master clear and run for each additional data block on tape.